# Memristors and Nonlinear Programming

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- Areas of interest:
    - Nonlinear Dynamics (Circuits). Specifically: chaotic circuits and memristors
    - Embedded (FPGA) Systems and Education

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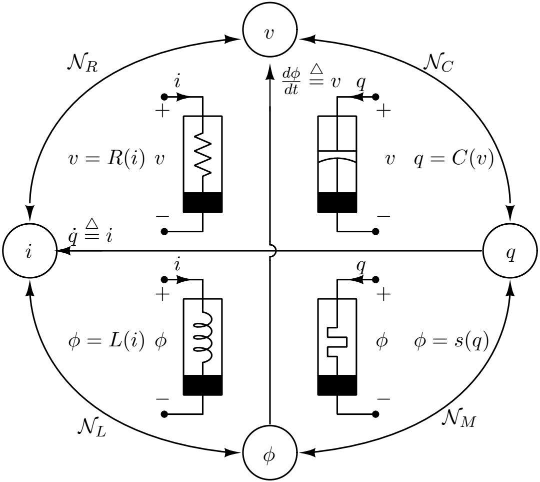
  - Conclusion and Q/A

# Fundamental Circuit Variables and Elements



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- Eq. (2) defines an ideal memristor (Josephson junctions)
- Generalization to a nonideal memristor:

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- Discharge tubes (internal state $x$ = number of conduction electrons $n$):

$$v = M(n)i \tag{4}$$

$$\frac{dn}{dt} = -\beta n + \alpha M(n)i^2 \tag{5}$$

# Memristive Models of RRAM

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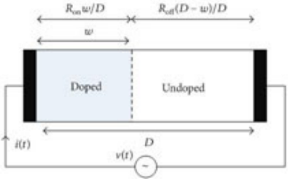

$$M(w(t)) = R_{on}\frac{w(t)}{D} + R_{off}\left(\frac{D-w(t)}{D}\right) \tag{6}$$

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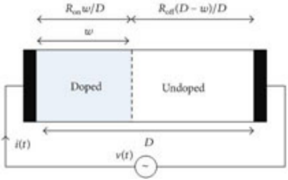

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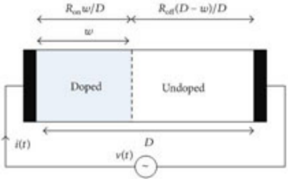

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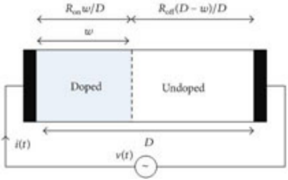

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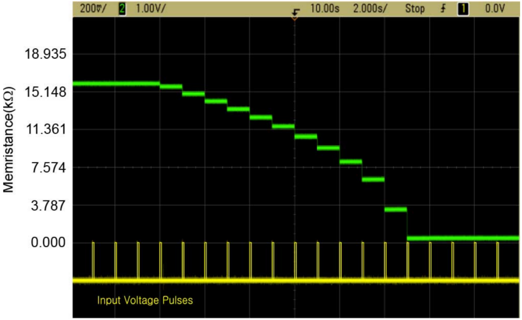
- Usually, $R_{off} >> R_{on}$

# Memristive Models of RRAM

- Changing memristance for input current pulses



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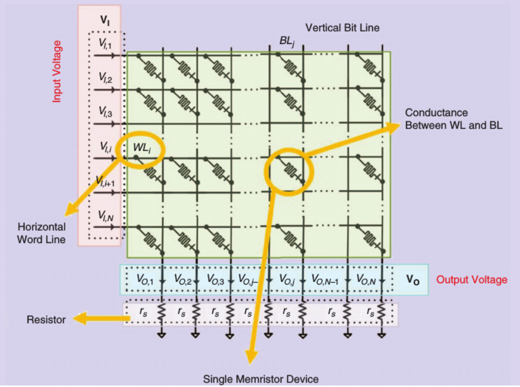
- However, a variety of fabrication challenges associated with RRAM (discussed in analog emulation of memristors)

# Memristor Crossbar Array Schematic



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$$\begin{bmatrix} V_{O,1} \\ \vdots \\ V_{O,M} \end{bmatrix} = \begin{bmatrix} \frac{g_{1,1}}{g_s + \sum\limits_{k=1}^{N} g_{1,K}} & \frac{g_{1,2}}{g_s + \sum\limits_{k=1}^{N} g_{1,K}} & \cdots & \frac{g_{1,N}}{g_s + \sum\limits_{k=1}^{N} g_{1,K}} \\ \vdots & \vdots & \vdots & \vdots \\ \frac{g_{M,1}}{g_s + \sum\limits_{k=1}^{N} g_{1,K}} & \frac{g_{M,2}}{g_s + \sum\limits_{k=1}^{N} g_{1,K}} & \cdots & \frac{g_{M,N}}{g_s + \sum\limits_{k=1}^{N} g_{1,K}} \end{bmatrix} \begin{bmatrix} V_{I,1} \\ \vdots \\ V_{I,N} \end{bmatrix} \tag{7}$$

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- Primary challenges in memristor crossbar array technology: scalability (addressed by using arbiters), process-variablity (hot topic of research), negative coefficients...

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- Mathematical "trick" of auxiliary variables in defining:
    - $\tilde{N}$: number of nonzero columns of $-\mathbf{C}_-$
    - $\mathbf{B} \in \mathbb{R}^{N \times \tilde{N}}$: nonzero columns of $-\mathbf{C}_-$
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- Usually $\tilde{N} << N$, size of resulting memristor crossbar array is $(N + \tilde{N}) \times (N + \tilde{N})$

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$$
\begin{aligned}
\mathbf{C} &= \begin{bmatrix} 1 & -3 & 0 \\ 0 & -0.75 & 4 \\ -2 & -5 & 6 \end{bmatrix} \\
&= \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 4 \\ 0 & 0 & 6 \end{bmatrix} - \begin{bmatrix} 0 & 3 & 0 \\ 0 & 0.75 & 0 \\ 2 & 5 & 0 \end{bmatrix} \\
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&= (\mathbf{C}_+ - (\mathbf{BD}))
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- Now, a variety of nonlinear programming problems can be mapped onto the memristor crossbar array...

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    - Constraint functions: timing threshold, device area, total area etc.

# Convex Optimization

- Mathematically ($f_0$: objective function, $\mathbf{f}_i$: constraint function(s) $f_0, \mathbf{f}_i : \mathbb{R}^n \rightarrow \mathbb{R}$):

$$\text{minimize} : f_0(\mathbf{x}) \tag{11}$$

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- We have a convex optimization problem iff $f_0, \mathbf{f}_i$ are convex:

$$f_k(\alpha\mathbf{x} + \beta\mathbf{y}) \leq \alpha f_k(\mathbf{x}) + \beta f_k(\mathbf{y}) \tag{13}$$

with $\alpha + \beta \geq 1, \alpha \geq 0, \beta \geq 0$

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- ADMM : Alternative Direction Method of Multipliers - decompose optimization variable into two simpler groups
- One of the main steps in ADMM involves solving the optimization problem:

$$\text{minimize}: \frac{\rho}{2}\|\mathbf{x}-\alpha\|_2^2 \tag{14}$$

$$\text{subject to}: \mathbf{G}\mathbf{x}=\mathbf{h} \tag{15}$$

where: $\mathbf{x} \in \mathbb{R}^n$ is the optimization variable, $\alpha$ is a "coupling" parameter, $\mathbf{G} \in \mathbb{R}^{l\times n}$ and $\mathbf{h} \in \mathbb{R}^l$ are parameters.

# ADMM Using the Memristor Crossbar Array

- Using the Karush-Kuhn-Tucker (KKT) necessary and sufficient conditions, we get the following equivalent equation to solve:

$$\rho(\mathbf{x} - \alpha) + \mathbf{G}^T\lambda = \mathbf{0} \tag{16}$$

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- The system in Eq. (18) can be efficiently mapped to memristor crossbars by configuring their memristance values according to $\mathbf{C} = \begin{bmatrix} \rho\mathbf{I} & \mathbf{G}^T \\ \mathbf{G} & \mathbf{0} \end{bmatrix}$

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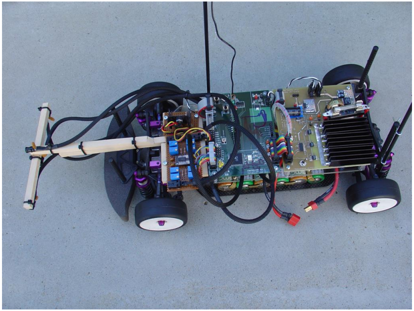

- NATCAR, Berkeley EECS 192

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- ...there is a need for robust (analog) emulators

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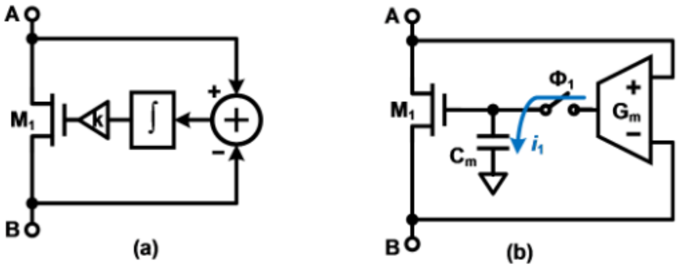
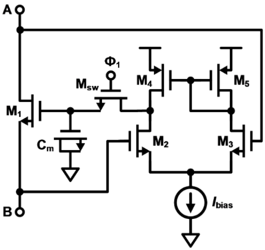
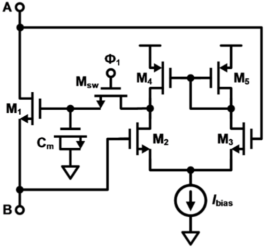


# CMOS-based Analog Emulation of Memristor RRAM: Implementation



$$
\begin{aligned}
I &\approx K_n \frac{W}{L}\left(V_G - V_{C_M} - V_{T_N}\right)\cdot V_{AB} \\
&= K_n \frac{W}{L}\left(x - V_{C_M} - V_{T_N}\right)\cdot V_{AB} \qquad (19)
\end{aligned}
$$

# CMOS-based Analog Emulation of Memristor RRAM: Implementation



$$
\begin{aligned}
I &\approx K_n \frac{W}{L}\left(V_G - V_{C_M} - V_{T_N}\right)\cdot V_{AB} \\
&= K_n \frac{W}{L}\left(x - V_{C_M} - V_{T_N}\right)\cdot V_{AB} \qquad (19)
\end{aligned}
$$

$$
\begin{aligned}
\dot{x} &= \frac{G_M(V_{AB})}{C_M} \\
&= f(V_{AB}) \qquad (20)
\end{aligned}
$$

# Conclusion, Q/A and References

- Ongoing research:
  - Implement convex optimization problems, say MLCP, via ADMM on memristor crossbar array (work jointly done with TCNJ faculty (Dr. Adegbege) and students (Paul B., Jake B., Matt K.)):
    - Simulation framework for memristors (crossbar array): QUCS (Quite Universal Circuit Simulator), MAPP (Berkeley Model and Algorithm Prototyping Platform)
    - Synthesize memristor crossbar array using Analog RRAM memristor emulator
    - Senior design project for AY 2018-2019
  - Memristive models for atrial fibrillation (with Dr. S. T. Mathew)
  - Noise induced chaos in the Muthuswamy-Chua system (with Dr. K. Ganesan and Dr. S. Banerjee)
- Questions?

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