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Memristor Modelling

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1. Introduction

The memristor was postulated as the fourth fundamental circuit element by Dr. Leon O. Chua in 1971 [2]. Figure 1 illustrates how the memristor completes the fundamental 2-terminal circuit elements in electrical engineering.

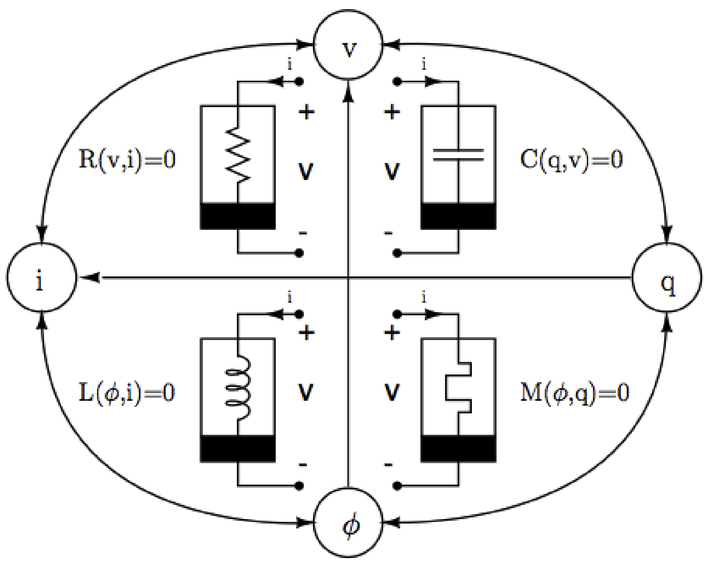


Figure 1. The four fundamental 2-terminal circuit elements [4].

This work provides a simple experimental setup for plotting the *v-i* pinched-hysteresis fingerprint of an **ubiquitous physical memristor (the discharge tube)** and hence confirming the fundamental theorem for memristor model-validation.

2. Method

The fundamental theorem for memristor modelling [3] is:

Theorem: Under a large-signal sinusoidal current excitation, the Lissajous figure associated with the periodic voltage response $v_M(t)$ and the excitation current $i_M(t)$ is generally a double-valued function which passes through the origin.

For a proof, please refer to [3]. Figure 2 shows a very simple circuit that helps us plot the *v-i* of a discharge tube.

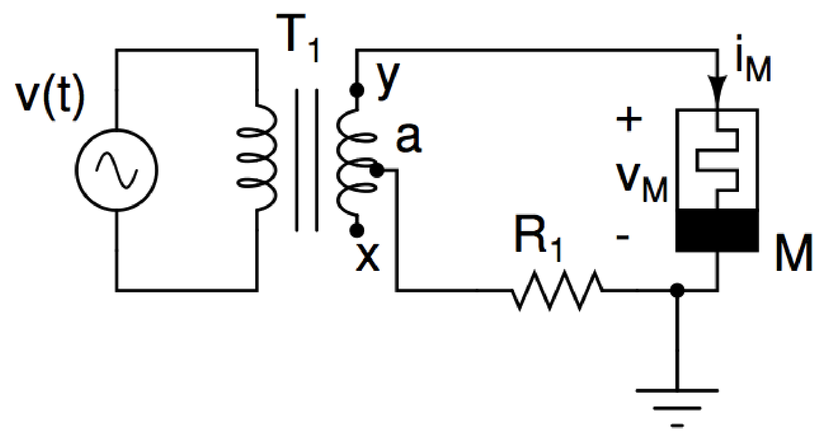


Figure 2. A Gaseous (Neon) Tube Transformer based setup for plotting the *v-i* characteristic of adischarge tube at 60 Hz.

3. Results

The definition of a current-controlled memristor and the memristive model of the discharge tube [3] is shown in Eqs. (1) through (4).

$$v = R(x,i)i \quad (1)$$

$$x' = f(x,i) \quad (2)$$

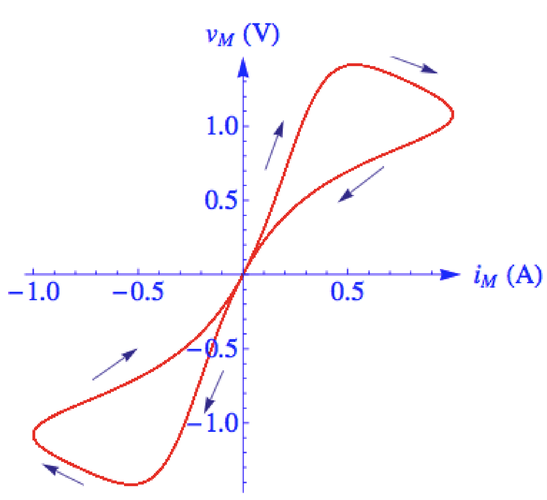
$$v = M(n)i \quad (3)$$

$$n' = -\beta n + \alpha M(n) i^2 \quad (4)$$

$M(n) = F/n, \alpha, \beta$ and F are parameters depending on the dimensions of the tube and gas fillings. n is the number of conduction electrons. Figures 3, 4 and 5 show the Mathematica simulation versus physical experimental results.

Using the setup in Figure 2, we can also investigate the effects of parasitic circuit elements (inductors in series and capacitors in parallel). Physically, the presence of these circuit elements will cause the memristor *v-i* to become un-pinched at the origin.

The main concept behind the effects of parasitic circuit elements is that current lags (leads) voltage by $\pi/2$ in a purely inductive (capacitive) circuit.



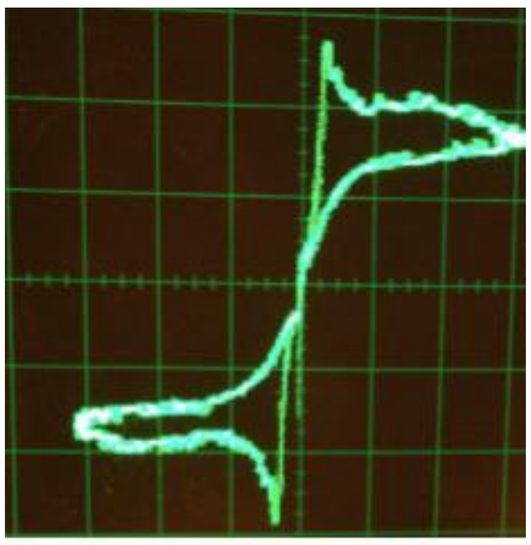
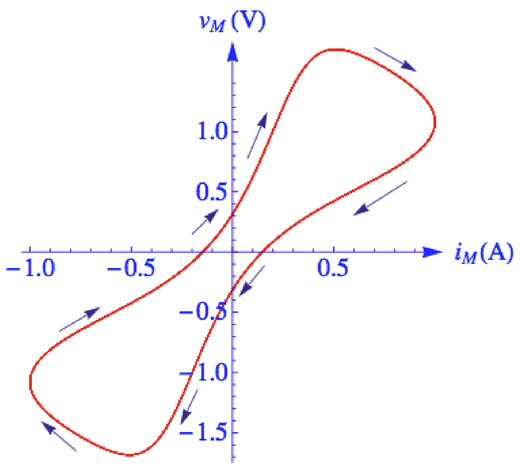


Figure 3. Simulation versus experimental result for memristor pinched-hysteresis (Lissajous) figure. $\dot{v}_M, \dot{i}_M$ are indicated on the plot. Parameters used for simulation: $\beta = 0.1, \alpha = 0.1, F = 1, \omega = 0.063$ The discharge tube is a Phillips 15 W F15T8.



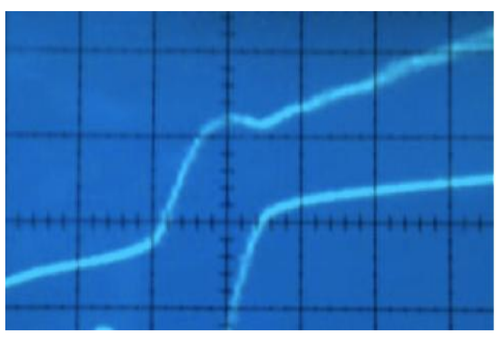
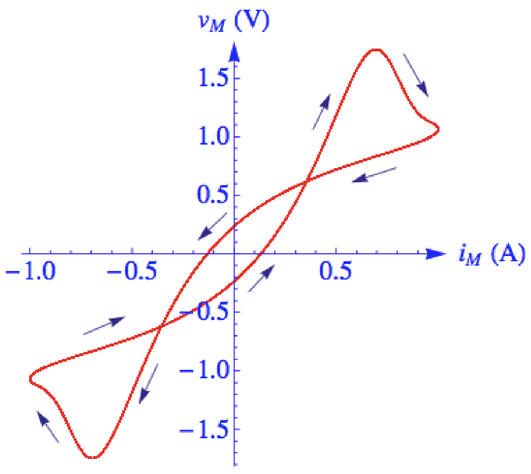


Figure 4. Simulation versus experimental result for memristor pinched-hysteresis (Lissajous) figure. For simulation, we used a 5 H inductor. For the physical setup, we used a 300 H inductor and "zoomed-in" at the origin since the transformer has a measured secondary inductance of 1400 H at 60 Hz.



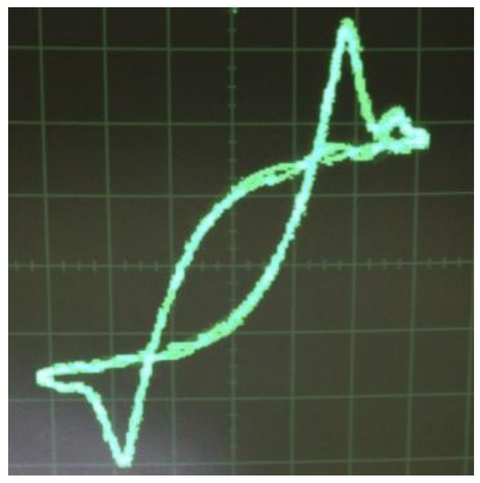


Figure 5. Simulation versus experimental result for memristor pinched-hysteresis (Lissajous) figure. For simulation, we used a 1 F capacitor; for the physical experiment, we show a 100 nF capacitor in parallel.

4. Discussions and Conclusions

In this work, we showed a simple experimental setup to plot the Lissajous *v-i* of a physical memristor – the discharge tube. We also illustrated the deviation of the pinched-hysteresis loop from the origin, in the presence of parasitic components.

One improvement to the circuit could be to make a variable frequency input, to confirm other memristor fingerprints, such as decrease in hysteresis lobe area with increasing frequency [1].

The physical memristor that we used has a non-transversal pinched-hysteresis loop [1]. A natural extension of this work would be for memristors with transversal pinched-hysteresis loops [1].

References

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Poster template reference: 2013 IEEE Thailand Student Conference on Senior Capstone Project