

Nonlinear Dynamics and Embedded FPGA Systems

July 10th 2014

Bharathwaj “Bart” Muthuswamy
Assistant Professor of Electrical Engineering
Milwaukee School of Engineering (MSOE)

muthuswamy@msoe.edu

<http://www.harpgroup.org/muthuswamy/>

BS (2002), MS (2005) and PhD (2009) from the University of California, Berkeley
PhD Advisor: Dr. Leon O. Chua (co-advised by Dr. Pravin P. Varaiya)

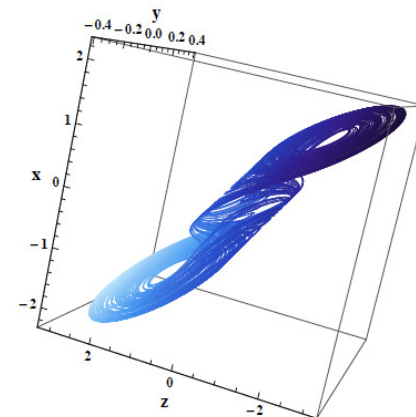
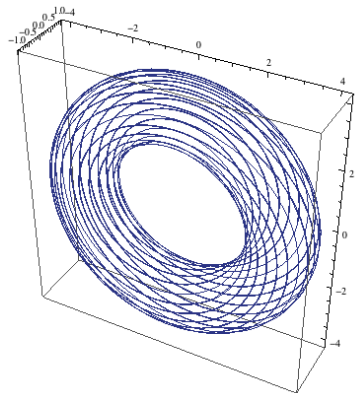
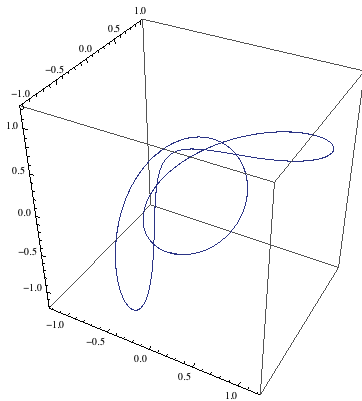
What do I work on?

Nonlinear Dynamical Systems and Embedded Systems

- Physical Memristors: discharge tubes, PN junctions and Josephson Junctions
(MSOE; IIT Chennai; University of Western Australia, Perth, Australia; Vellore Institute of Technology (VIT), Vellore, India)
- Applications and Mathematical properties of the Muthuswamy-Chua system
(MSOE; VIT; University of Western Australia; AGH-University of Science and Technology, Poland)
- Applications of Chaotic Delay Differential Equations using Field Programmable Gate Arrays (FPGAs)
(MSOE; VIT; University Putra Malaysia, Malaysia)
- Pattern Recognition Using Cellular Neural Networks on FPGAs
(MSOE; VIT; Altera Corporation)

Education

- Nonlinear Dynamics at the undergraduate level (with folks from all over the world ☺)



Primary Goal of this Talk

Overview of my research interests

Outline

I. Background

1. The Question of Applications
2. The Science and Art of Device Modeling

II. The Memristor

1. The Fundamental Circuit Elements
2. Properties of the Memristor
3. Memristive Devices
4. Memristor Emulator
5. Physical Memristors
 - a. Non-ideal Memristors:
 - i. Discharge tube
 - ii. Junction diode
 - b. Ideal memristor:
 - i. Josephson junction

III. The Muthuswamy-Chua System (Circuit)

IV. FPGA Based Nonlinear Dynamics

1. Chaotic Systems
2. Pattern (Image) Recognition

V. Conclusions, Current (future) work and References

The Question of Applications

Scientific discoveries and inventions have only been achieved by those who went in pursuit of them without any applications in mind

- Max Planck

Who was Max Planck?

The Science and Art of Device Modeling

We first have to understand that a circuit model is not an equivalent circuit of a device since no physical device can be exactly mimicked by a circuit or mathematical model [9]. In fact, depending on the application (e.g., frequency of operation), a given device may have many distinct physical models [9]. There is no "best model" for all occasions. The best model in a given situation is the simplest model capable of yielding realistic solutions [9]. Thus device modeling is both an art (physical device equation formulation) and science (nonlinear network synthesis).

Outline

I. Background

1. The Question of Applications
2. The Art and Science of Device Modeling

II. The Memristor

1. The Fundamental Circuit Elements
2. Properties of the Memristor
3. Memristive Devices
4. Memristor Emulator
5. Physical Memristors
 - a. Non-ideal Memristors:
 - i. Discharge tube
 - ii. Junction diode
 - b. Ideal memristor:
 - i. Josephson junction

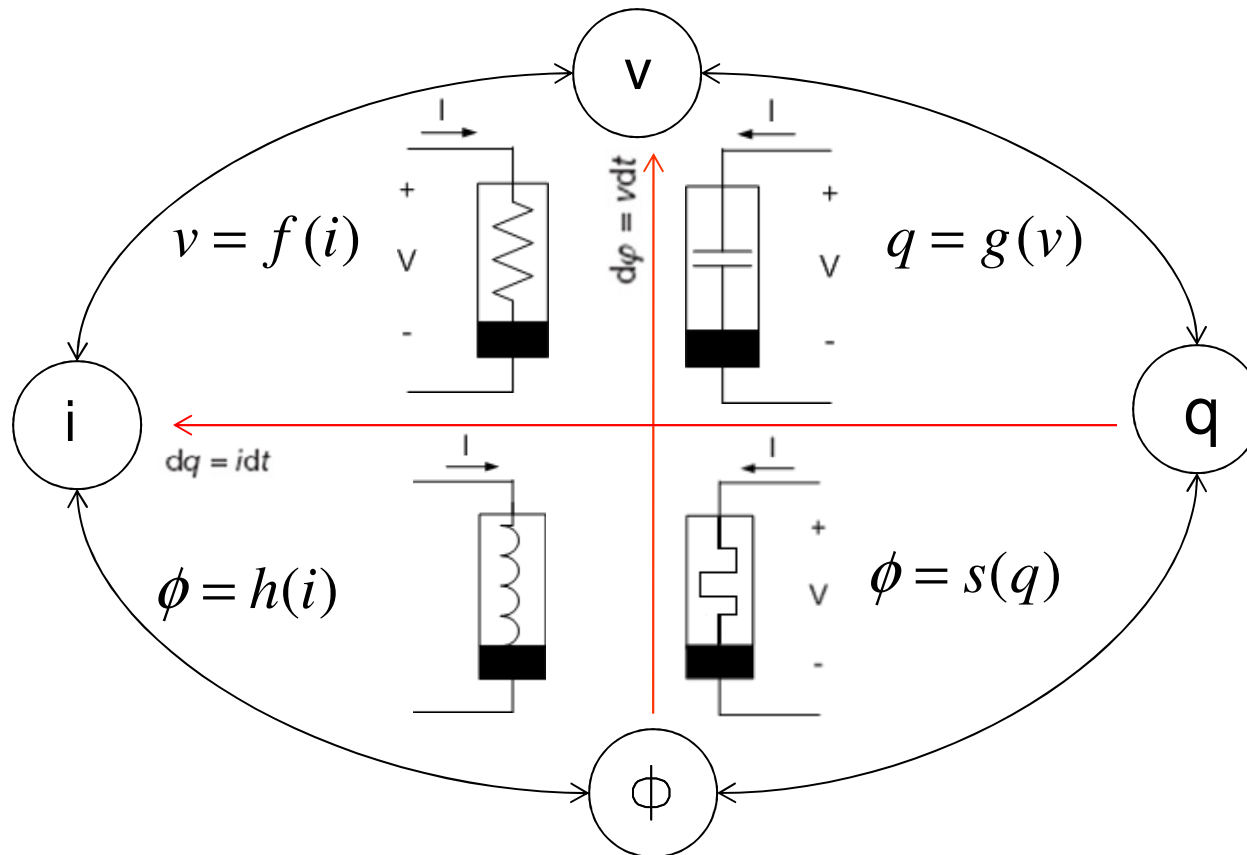
III. The Muthuswamy-Chua System (Circuit)

IV. FPGA Based Nonlinear Dynamics

1. Chaotic Systems
2. Pattern (Image) Recognition

V. Conclusions, Current (future) work and References

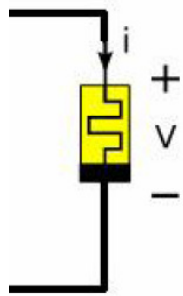
The Fundamental Circuit Elements



Memristors were first postulated by Leon. O Chua in 1971 [2]. In 2008, researchers at HP claimed to have found the “missing” memristor [11].

Properties of the Memristor [2] [4]

Circuit symbol: A memristor defines a *relation* of the form: $g(\phi, q) = 0$ (1)

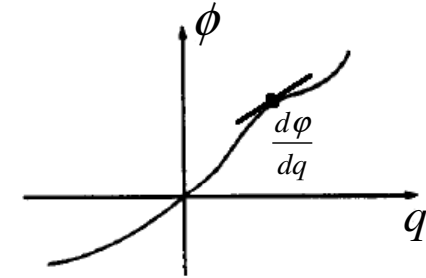


If g is a single-valued function of charge (flux), then the memristor is charge-controlled (flux-controlled)

Memristor i-v relationship:

$M(q(t))$ is the incremental memristance

$$v(t) \triangleq \frac{d\phi}{dt} = \frac{d\phi}{dq} \frac{dq}{dt} \triangleq M(q(t))i(t) \quad (2)$$



Q1: Why is the memristor called “memory resistor”?

Because of the definition of memristance: $v(t) = M(q(t))i(t) = M\left(\int_{-\infty}^t i(\tau)\right)i(t)$ (3)

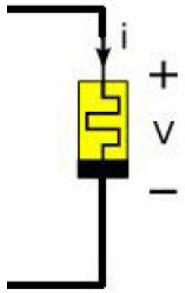
Q2: Why is the memristor not relevant in linear circuit theory?

1. If $M(q(t))$ is a constant: $v(t) = M(q(t))i(t) = Mi(t) = Ri(t)$ (4)

2. Principle of superposition is not* applicable. Proof:

$$M\left(\int_{-\infty}^t (i_1 + i_2)(\tau)\right)(i_1 + i_2)(t) = M\left(\int_{-\infty}^t (i_1)(\tau) + \int_{-\infty}^t (i_2)(\tau)\right)(i_1 + i_2)(t) \neq M\left(\int_{-\infty}^t (i_1)(\tau)\right)i_1(t) + M\left(\int_{-\infty}^t (i_2)(\tau)\right)i_2(t)$$

Memristive Devices [4]



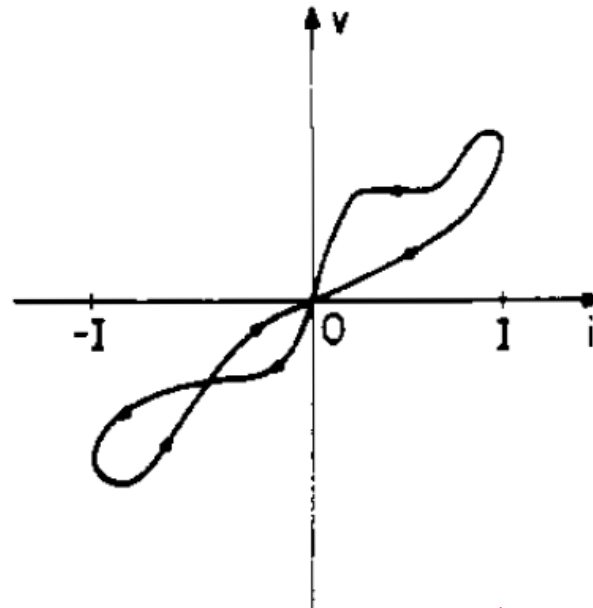
$$\begin{aligned} v &\triangleq R(\vec{z}, i)i \\ \dot{\vec{z}} &= f(\vec{z}, i) \end{aligned} \quad (5)$$

$$\xrightarrow{\vec{z} \triangleq q, R(\vec{z}, i) \triangleq M(q)} \begin{aligned} v &\triangleq M(q)i \\ \dot{q} &= i \end{aligned} \quad (6)$$

The functions R and f are defined as:

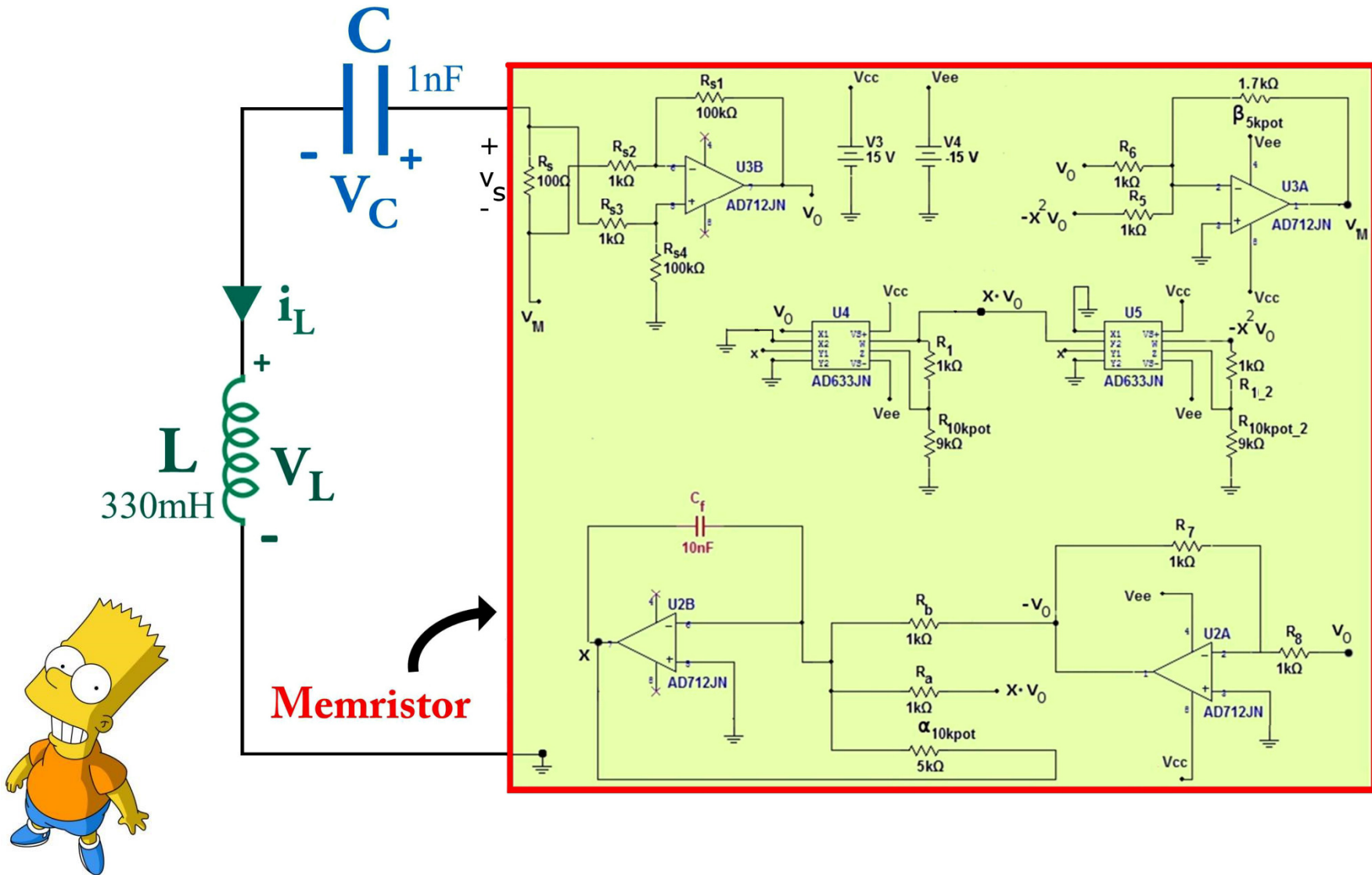
$$R: \mathbb{R}^n \times \mathbb{R} \rightarrow \mathbb{R}$$

$$f: \mathbb{R}^n \times \mathbb{R} \rightarrow \mathbb{R}^n$$

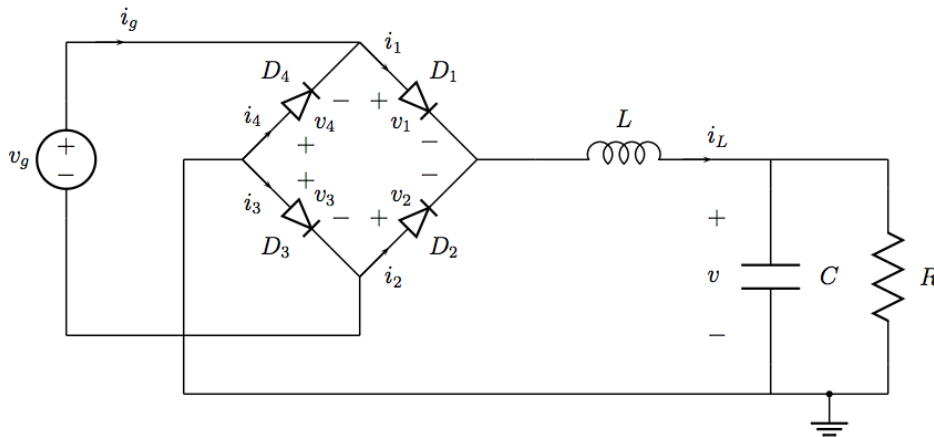


In Eq. (5), $R(\vec{z}, i) \not\rightarrow \infty$

Memristor Emulation [8]



Memristor Emulation : Passive Elements only [5]



$$v_1 = nV_T \ln \left(\frac{i_L + 2I_S}{2I_S \exp\left(-\frac{v_g}{2nV_T}\right) \cosh\left(\frac{v_g}{2nV_T}\right)} \right) \quad (7)$$

$$i_g = (i_L + 2I_S) \tanh\left(\frac{v_g}{2nV_T}\right) \quad (8)$$

$$\frac{d\mathbf{x}}{dt} = f(\mathbf{x}, u, t)$$

$$y = g(\mathbf{x}, u, t)u \quad (9)$$

$$f(\mathbf{x}, u, t) = \left[\gamma \left(u - x_1 - 2 \ln \left(\frac{x_2 + 2}{2 \exp\left(-\frac{u}{2n}\right) \cosh\left(\frac{u}{2n}\right)} \right) \right) \right] \quad (10)$$

$$g(\mathbf{x}, u, t) = (x_2 + 2) \frac{\sum_{m=0}^{\infty} \frac{\left(\frac{u}{2n}\right)^{2m}}{(2m+1)!}}{\sum_{m=0}^{\infty} \frac{\left(\frac{u}{2n}\right)^{2m}}{(2m)!}}, \quad (11)$$

$$x_1 = v (V_T)^{-1}$$

$$x_2 = i_L (I_S)^{-1}$$

$$u = v_g (V_T)^{-1}$$

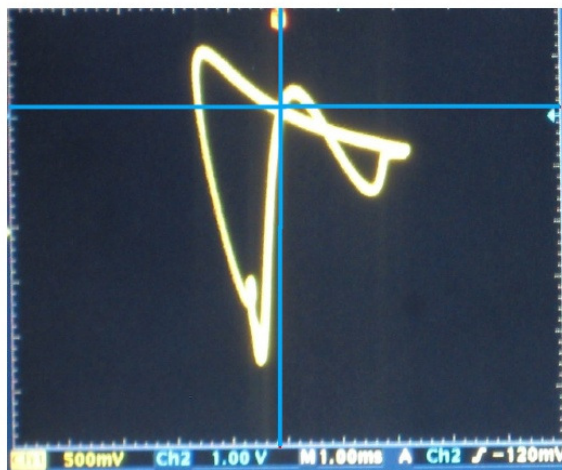
$$y = i_g (I_S)^{-1}$$

$$\tau = t (t_0)^{-1}$$

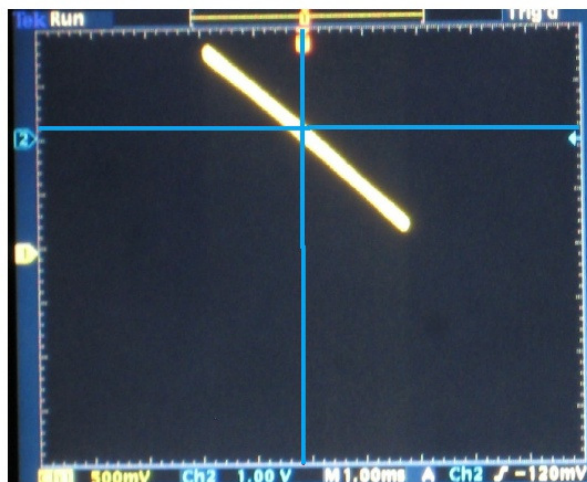
$$t_0 = 2\pi (\omega_0)^{-1}$$

$$\omega_0 = [(LC)^{-1} - (RC)]^{\frac{1}{2}}$$

Memristor Emulators – Pinched Hysteresis Loops [8] [5]



From [3], pinched-hysteresis for 3 kHz sinusoidal input



From [3], pinched-hysteresis for 35 kHz sinusoidal input

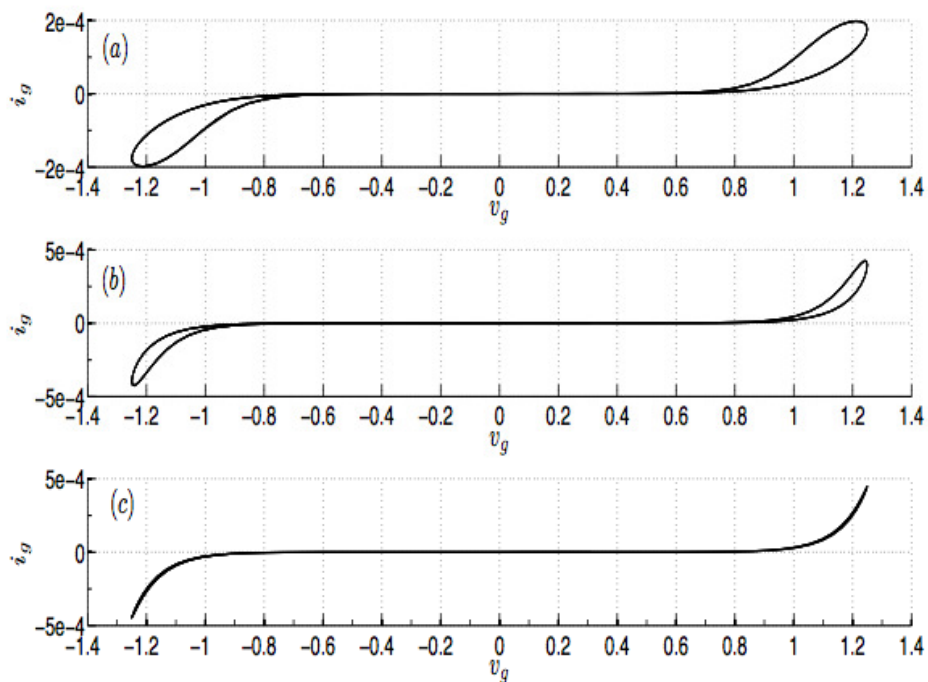


Fig. 3 Current-voltage characteristics observed in numerical simulations of the mathematical model of the proposed circuit for a sine-wave input with f set to 10 (plot (a)), 100 (plot (b)) and 1000 Hz (plot (c)).

From [4]

Non-ideal Memristor : Discharge Tube [9]

$$v = M(n)i$$

$$\dot{n} = -\beta n + \alpha M(n)i^2 \quad (12)$$

$$M(n) \triangleq \frac{F}{n} \quad (13)$$

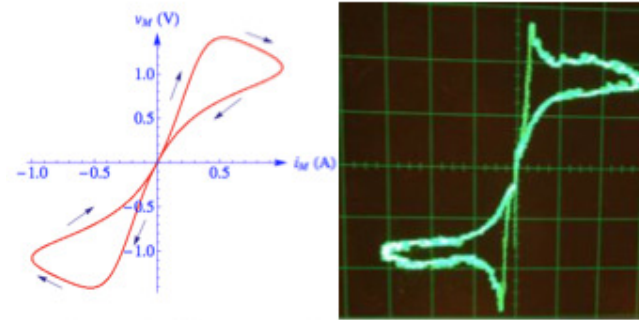
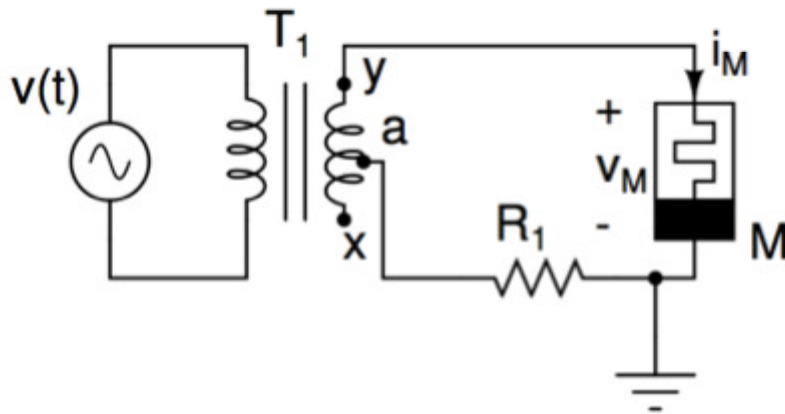


Figure 3. Simulation versus experimental result for memristor pinched-hysteresis (Lissajous) figure. v_M, i_M are indicated on the plot. Parameters used for simulation: $\beta = 0.1, \alpha = 0.1, F = 1, \omega = 0.063$ The discharge tube is a Phillips 15 W F15T8.

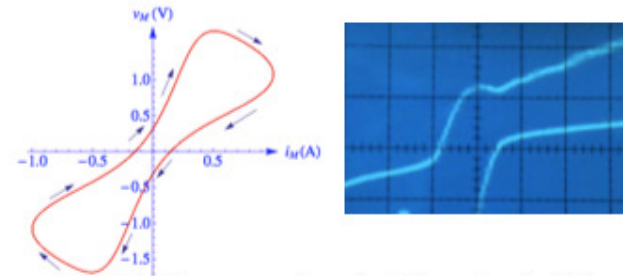


Figure 4. Simulation versus experimental result for memristor pinched-hysteresis (Lissajous) figure. For simulation, we used a 5 H inductor. For the physical setup, we used a 300 H inductor and "zoomed-in" at the origin since the transformer has a measured secondary inductance of 1400 H at 60 Hz.

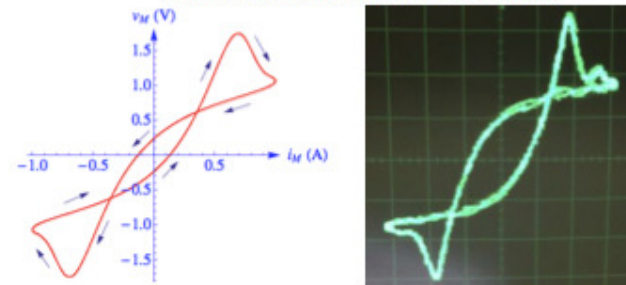
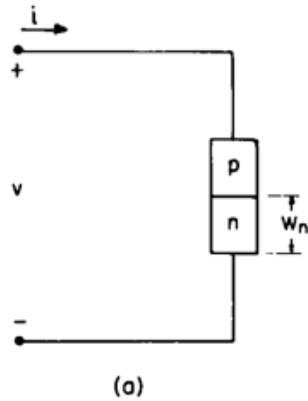


Figure 5. Simulation versus experimental result for memristor pinched-hysteresis (Lissajous) figure. For simulation, we used a 1 F capacitor; for the physical experiment, we show a 100 nF capacitor in parallel.

Non-ideal Memristor : Junction Diode [3]

Simulation of $R_m(q_m)$ for memristive model of a pn junction diode (Ref. : A Memristive Circuit Model for P-N Junction Diodes, Chua, L. O. and Tseng, Chong-Wei. International Journal of Circuit Theory and Applications, Vol. 2, 367-389 (1974))

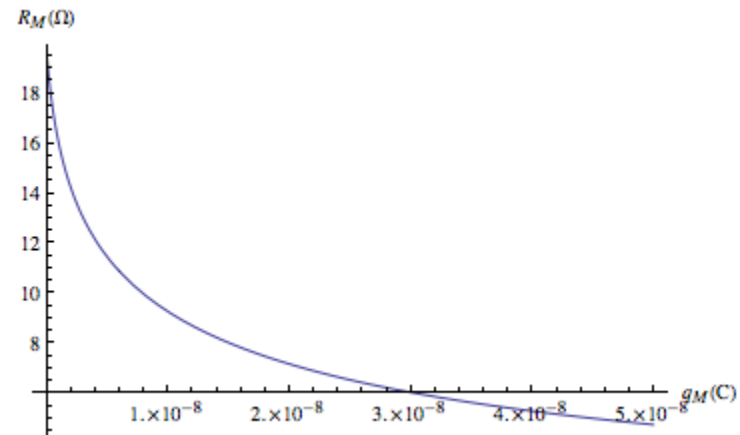
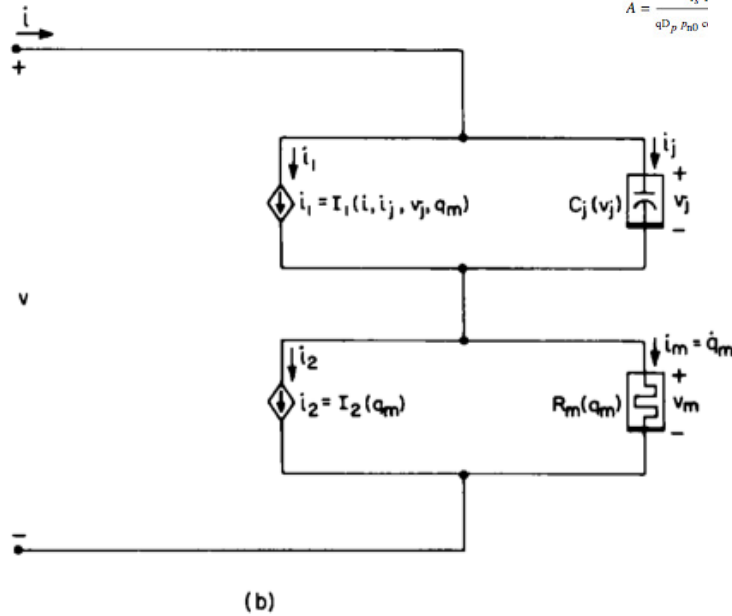


Parameters :

- $N_D = 10^{15} \text{ cm}^{-3}$ (donor concentration)
- $\mu_n = 1350 \text{ cm}^2 / \text{V}\cdot\text{sec}$ (electron mobility)
- $\mu_p = 480 \text{ cm}^2 / \text{V}\cdot\text{sec}$ (hole mobility)
- $I_S = 0.5 * 10^{-12} \text{ A}$ (diode saturation current)
- $\tau_p = 10^{-7} \text{ sec}$ (hole recombination life time)
- $V_T = 26.047 \text{ mV}$ (thermal voltage)
- $D_p = \mu_p V_T$ (hole diffusion constant)
- $L_p = \sqrt{D_p \tau_p}$ (hole diffusion length)
- $w_n = 5 L_p$ (width of the n - type region or base width)
- $T = 300 \text{ K}$ (Ambient temperature)
- $\psi_0 = 0.9 \text{ V}$ (barrier potential)
- $n_{n0} = N_D$ (approximately) (equilibrium electron concentration in the n - type region)
- $n_i = 8.367 * 10^8 \text{ cm}^{-3}$ (@ 300 K) (intrinsic concentration)
- $p_{p0} = \frac{(n_i)^2}{n_{n0}} = 2.1 * 10^5$ (equilibrium hole concentration in the p - type region)
- $A = \frac{I_s l}{q^2 D_p p_{p0} \sigma}$

$$\sigma [x, q_m] := q * \mu_n * n_{n0} + q * \mu_p * \left(p_{p0} + \frac{q_m}{A * q * L_p} * \left(\frac{\text{Sinh} \left[\frac{W_n}{L_p} \right]}{\text{Cosh} \left[\frac{W_n}{L_p} \right] - 1} \right) + \left(\text{Cosh} \left[\frac{x}{L_p} \right] - \text{Coth} \left[\frac{W_n}{L_p} \right] * \text{Sinh} \left[\frac{x}{L_p} \right] \right) \right) \quad (14)$$

$$R_m [q_m] := \frac{1}{A} * \int_0^{W_n} \frac{1}{\sigma [x, q_m]} dx \quad (15)$$



Ideal Memristor : Josephson Junction [6] [10]

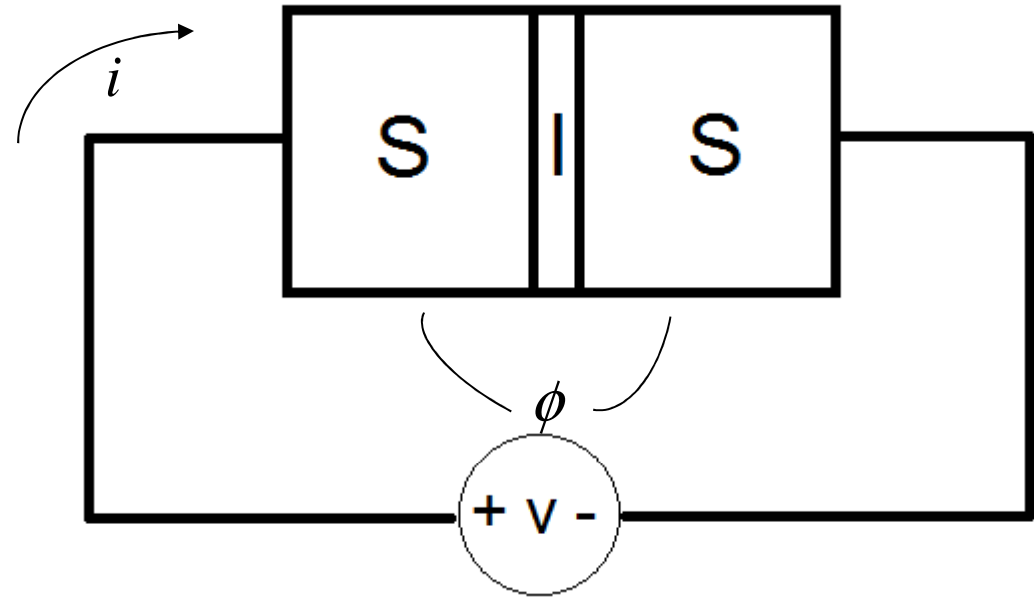
$$E = h \cdot \nu \quad (16)$$

$$= h \frac{\omega}{2\pi}$$

$$= \hbar \frac{d\phi}{dt}$$

$$2e^- \nu = \hbar \frac{d\phi}{dt}$$

$$\frac{2e^-}{\hbar} \nu = \frac{d\phi}{dt}$$



$$\frac{d\phi}{dt} = \frac{2e^-}{\hbar} \nu \quad (17)$$

Ideal Memristor : Josephson Junction (contd.)

Suppose $v = 1 \text{ uV}$. f (in Hz) for the Josephson junction $\approx 0.482 \text{ GHz!}$

$$\frac{d\phi}{dt} = \frac{2e^-}{\hbar} (1 \mu V)$$
$$\Rightarrow f = \frac{\frac{2e^-}{\hbar} (1 \mu V)}{2\pi} \approx 482 \text{ MHz}$$

$$\frac{d\Phi_B}{dt} = v$$

$$\Phi_B \triangleq \frac{\hbar}{2e^-} \phi = k\phi \quad (18)$$

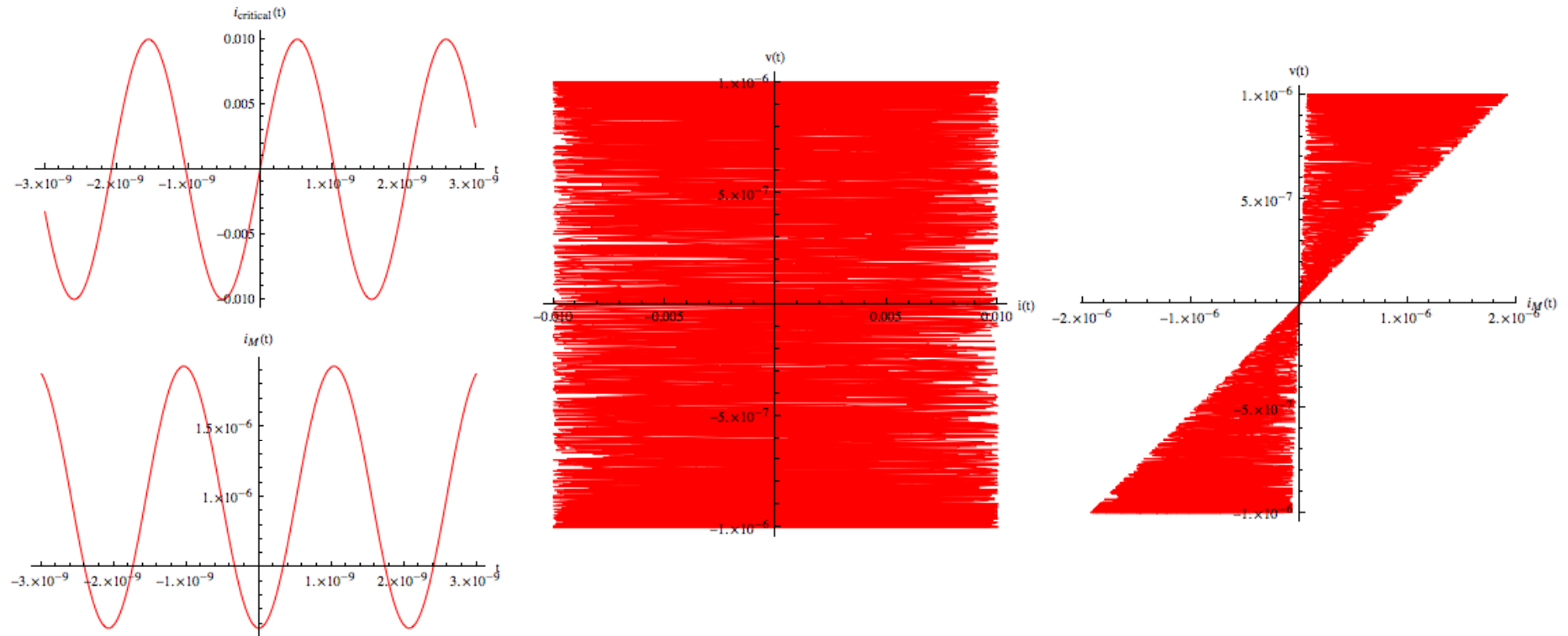
Ideal Memristor : Josephson Junction (contd.)

In fact, according to the microscopic theory (Josephson 1962), in the case in which V is constant and the transmission coefficient through the barrier for quasi-particles is small compared to unity, j_z is given by an expression of the form :

$$j_z = j_1(V) \sin \phi + \{\sigma_0(V) + \sigma_1(V) \cos \phi\} V. \quad . \quad . \quad . \quad (3.10)$$

$$I = I(v) \sin \left(\frac{2e^-}{\hbar} \Phi_B \right) + \left(\sigma_0(v) + \sigma_1(v) \cos \left(\frac{2e^-}{\hbar} \Phi_B \right) \right) v \quad (19)$$

Ideal Memristor : Josephson Junction (contd.)



On 14 Mar 2014, at 16:28, Bharathwaj Muthuswamy <muthuswamy@msoe.edu> wrote:

1. Is it even possible to isolate ONLY the $\cos(\phi)$ term in the Josephson junction?
2. Does it even make sense to ask if we can isolate the $\cos(\phi)$ term in the Josephson junction?

Thanks for your email. I think the answer is that the $\cos(\phi)$ term is non-zero only when there's a non-zero voltage, and then it would be oscillating at a very high frequency ($2eV/h$), which probably makes it unsuitable for your purposes.

Regards, Brian Josephson

Brian D. Josephson
Emeritus Professor of Physics, University of Cambridge
Director, Mind-Matter Unification Project
Cavendish Laboratory, JJ Thomson Ave, Cambridge CB3 0HE, UK
WWW: <http://www.tcm.phy.cam.ac.uk/~bdj10>
Tel. +44(0)1223 337260/337254

Outline

I. Background

1. The question of Applications
2. The Art and Science of Device Modeling

II. The Memristor

1. The Fundamental Circuit Elements
2. Properties of the Memristor
3. Memristive Devices
4. Memristor Emulator
5. Physical Memristors
 - a. Non-ideal Memristors:
 - i. Discharge tube
 - ii. Junction diode
 - b. Ideal memristor:
 - i. Josephson junction

III. The Muthuswamy-Chua System (Circuit)

IV. FPGA Based Nonlinear Dynamics

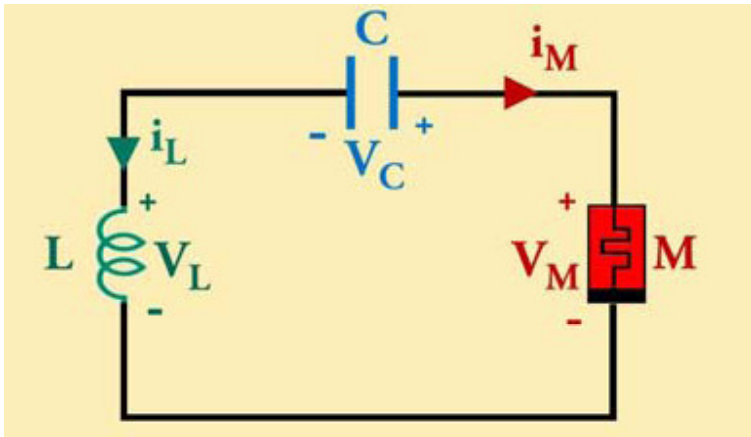
1. Chaotic Systems
2. Pattern (Image) Recognition

V. Conclusions, Current (future) work and References

The Muthuswamy-Chua Circuit [8]

$$v_M \triangleq R(z, i_M) i_M$$

$$\dot{z} = f(z, i_M)$$



Circuit equations:

$$\dot{v}_c = \frac{i_L}{C}$$

$$i'_L = \frac{-1}{L}(v_c + R(z, i_L) i_L)$$

$$\dot{z} \triangleq f(z, i_L) \quad (20)$$

System equations:

$$x \triangleq v_c, y \triangleq i_L \quad \dot{x} = \frac{y}{C}$$

$$y = \frac{-1}{L}(x + R(z, y)y) \quad (21)$$

$$\dot{z} = f(z, y)$$

Specifically:

$$\dot{x} = \frac{y}{C}$$

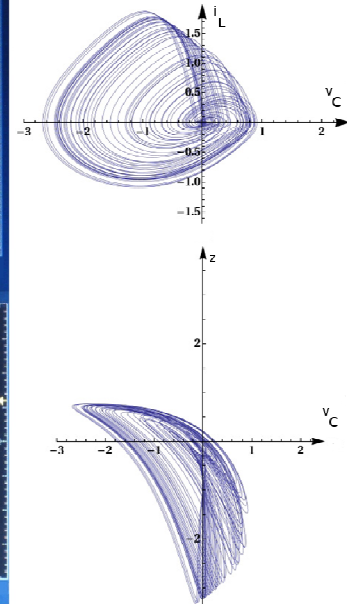
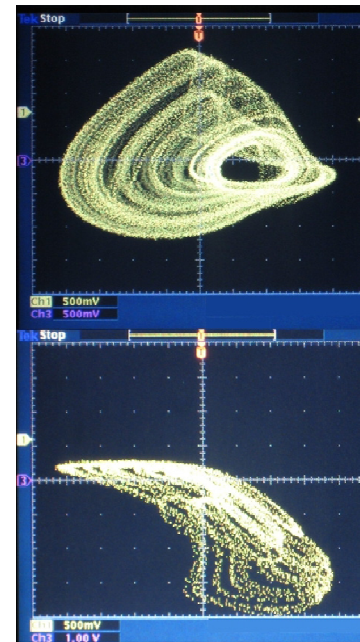
$$\dot{y} = \frac{-1}{L}(x + \beta(z^2 - 1)y) \quad (22)$$

$$\dot{z} = -y - \alpha z + yz$$

Parameters:

$$C=1, L=3$$

$$\beta = \frac{3}{2}, \alpha = \frac{3}{5}$$



Outline

I. Background

1. The question of Applications
2. The Art and Science of Device Modeling

II. The Memristor

1. The Fundamental Circuit Elements
2. Properties of the Memristor
3. Memristive Devices
4. Memristor Emulator
5. Physical Memristors
 - a. Non-ideal Memristors:
 - i. Discharge tube
 - ii. Junction diode
 - b. Ideal memristor:
 - i. Josephson junction

III. The Muthuswamy-Chua System (Circuit)

IV. FPGA Based Nonlinear Dynamics

1. Chaotic Systems
2. Pattern (Image) Recognition

V. Conclusions, Current (future) work and References

FPGA Based Nonlinear Dynamics: Chaotic Systems [12]

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, \mathbf{x}(t - \tau)) \quad (23)$$

$$\dot{x} = \mu \sin(x(t - \tau)) - \alpha x(t) \quad (24)$$

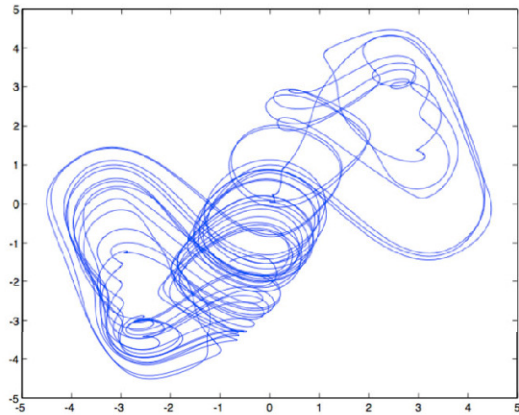
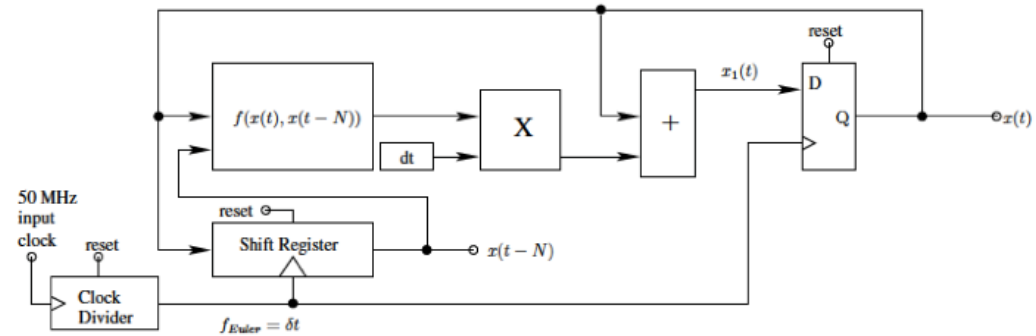
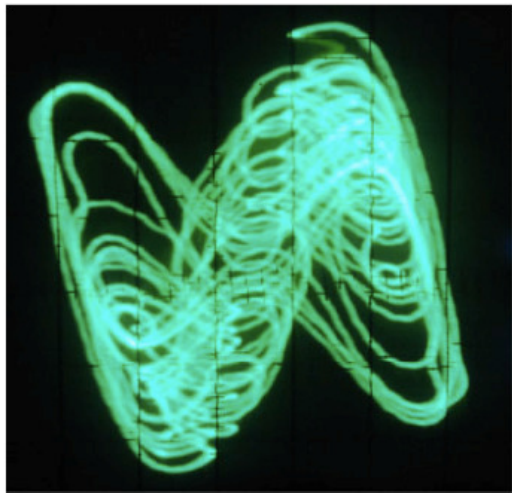
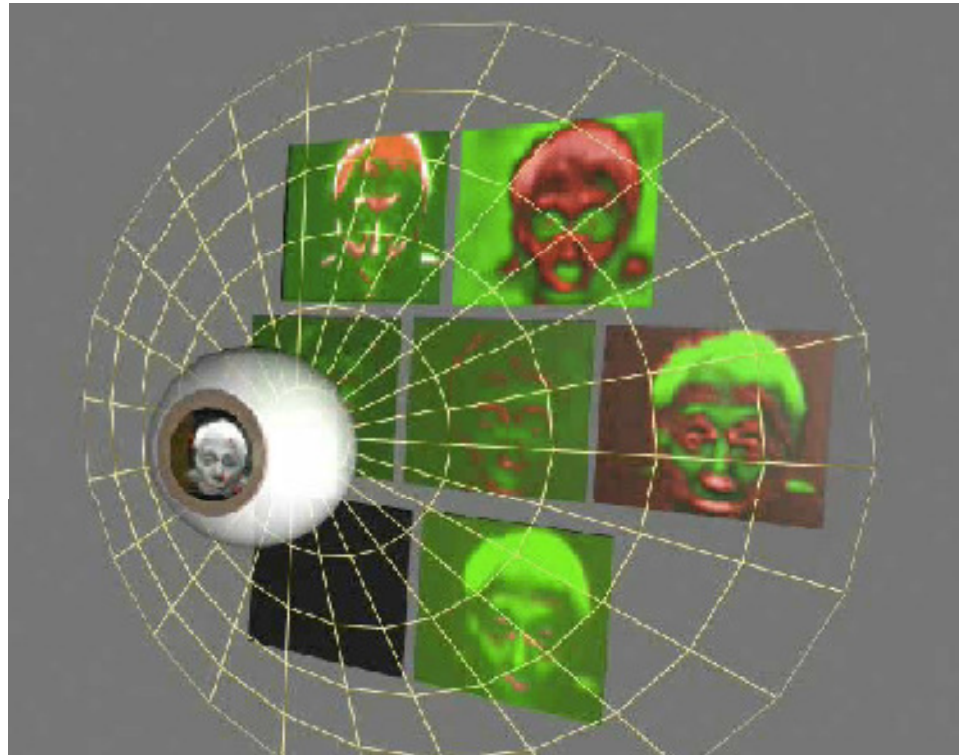


Fig. 5. Result from hardware co-simulation, plotted using XY graph in Simulink. y -axis is $x(t)$, x -axis is $x(t - \tau)$.



Flow Status	Successful - Tue Dec 03 21:55:49 2013
Quartus II 32-bit Version	12.0 Build 178 05/31/2012 SJ Full Version
Revision Name	DE2ChaoticDDEs
Top-level Entity Name	DE2ChaoticDDEs
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
▪ Total logic elements	18,268 / 114,480 (16 %)
Total combinational functions	16,788 / 114,480 (15 %)
Dedicated logic registers	8,977 / 114,480 (8 %)
Total registers	8977
Total pins	104 / 529 (20 %)
Total virtual pins	0
Total memory bits	70,559 / 3,981,312 (2 %)
Embedded Multiplier 9-bit elements	117 / 532 (22 %)
Total PLLs	1 / 4 (25 %)

FPGA Based Nonlinear Dynamics: Pattern (Image) Recognition



Utilize ideas behind the retinal hypercircuit (Werblin Lab, Berkeley) for recognition of hand-drawn circuit diagrams

Conclusions

- Overview of my research
 - Memristors
 - Chaos
 - FPGAs

Current and Future Work

1. Understanding v-i characteristics of discharge tube:
Circuit for plotting v-i (with Dr. Iu (UWA), Dr. Loo (HKP))
2. Chaos in Muthuswamy-Chua with discharge tube [1] (with Dr. Iu, Dr. Loo and Dr. Corinto (Politecnico di Torino))
3. Identifying ideal memristive behavior in the Josephson junction (with IIT-Chennai and VIT)
4. Complete SPICE model of junction diode with memristor (with Dr. Jevtic (MSOE))
 - Specifically for 3. and 4., use the idea of frequency-power formulae?
5. An electromagnetic field (physical) theory for memristors (with Dr. Jevtic and Dr. Thomas (MSOE)).
6. FPGA Based Nonlinear Dynamics: Pattern Recognition

References

1. Braun, T. et. al. "Observation of Deterministic Chaos in Electrical Discharges in Gases", *Physical Review Letters*, Vol. 59, No. 6, pp. 613-616, 1987.
2. Chua, L. O. "Memristor-The Missing Circuit Element". *IEEE Transactions on Circuit Theory*, Vol. CT-18, No. 5, pp. 507- 519. September 1971.
3. Chua, L. O. and Tseng, C. "A Memristive Circuit Model for P-N Junction Diodes". *Circuit Theory and Applications*. Vol. 2, pp. 367-389, 1974.
4. Chua, L. O. and Kang, S. M. "Memristive Devices and Systems". *Proceedings of the IEEE*, Vol. 64, No. 2, pp. 209- 223. February 1976.
5. Corinto, F. and Ascoli, A. "Memristive Diode Bridge with LCR Filter". *Electronics Letters*, Vol. 48, No. 14, pp.824–825, DOI: <http://dx.doi.org/10.1049/el.2012.1480>.
6. Josephson, B. "Supercurrents through Barriers". *Advances in Physics*, Vol. 14, No. 56, pp. 419 – 451, 1965.
7. Mader, U. and Horn, P. "A Dynamic Model for the Electrical Characteristics of Fluorescent Lamps", *IEEE Industrial Applications Society – Annual Meeting*, Vol. 2, pp. 1928 – 1934, 1992.
8. Muthuswamy, B. and Chua, L. O. "Simplest Chaotic Circuit". *International Journal of Bifurcation and Chaos*, vol. 20, No. 5, pp. 1567-1580. May 2010.
9. Muthuswamy, B. et. al. "Memristor Modelling". *Proceedings of the 2014 International Symposium on Circuits and Systems*, Melbourne, Australia, June 1st – 5th 2014.
10. Penfield, P. "Frequency Power Formulas for Josephson Junctions". MIT Technical Report – *Micrometer and Millimeter Wave Techniques*, QPR 113, 1973.
11. Strukov, D. B., Snider, G. S., Steward, D. R. and Williams, S. R. "The missing memristor found". *Nature*, vol. 453, pp. 81-83, 1st May 2008.
12. Valli, D. et. al. "Synchronization in Coupled Ikeda Delay Systems – Experimental Observations Using Field Programmable Gate Arrays". *European Physical Journal: Special Topics*. DOI: 10.1140/epjst/e2014-02144-8, 2014.

MANY THANKS TO DR. JEVTIC AND DR. THOMAS (MSOE)

Questions and Discussion...