Introduction to FPGAs (Field Programmable Gate Array) Latest Trends in FPGA Technology

Two Day Workshop on FPGA Programming for Beginners

Vellore Institute of Technology

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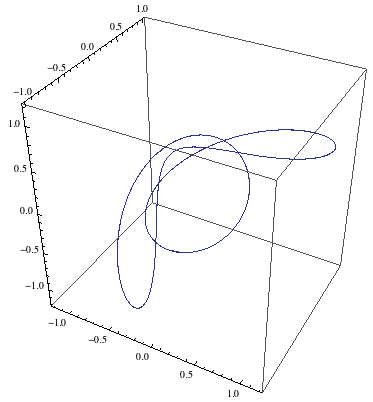
What *do* I work on?

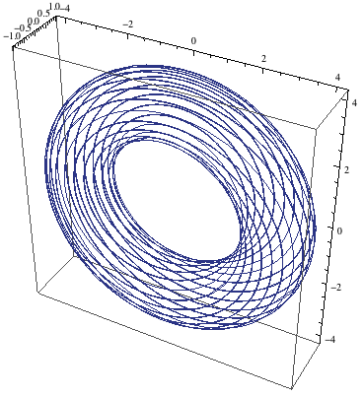
Nonlinear Dynamical Systems and Embedded Systems

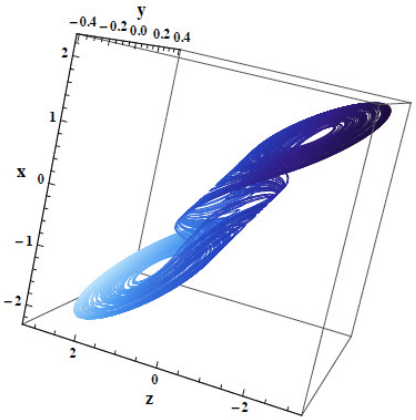
- Physical Memristors: discharge tubes, PN junctions and Josephson Junctions
  (MSOE; IIT Chennai; University of Western Australia, Perth, Australia; Vellore Institute of Technology (VIT), Vellore, India)
- Applications and Mathematical properties of the Muthuswamy-Chua system
  (MSOE; VIT; University of Western Australia; AGH-University of Science and Technology, Poland)
- Applications of Chaotic Delay Differential Equations using Field Programmable Gate Arrays (FPGAs)
  (MSOE; VIT; University Putra Malaysia, Malaysia)
- Pattern Recognition Using Cellular Neural Networks on FPGAs
  (MSOE; VIT; Altera Corporation)

Education

- Nonlinear Dynamics at the undergraduate level (with folks from all over the world ☺)







Outline

I. Prerequisites for understanding this workshop:
   1. *First course in digital combinational logic design
   2. Willingness to think and learn

II. A Brief History of FPGAs

III. Why FPGAs?

IV. Disadvantages of FPGAs

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VI. Conclusion and References

A Brief History of FPGAs

1. Originated from the programmable read-only memory and programmable logic devices industry of the 1970s [1].

2. Xilinx co-founders Ross Freeman and Bernard Vonderschmitt invented the first commercially viable FPGA in 1985 – the XC2064 [1].

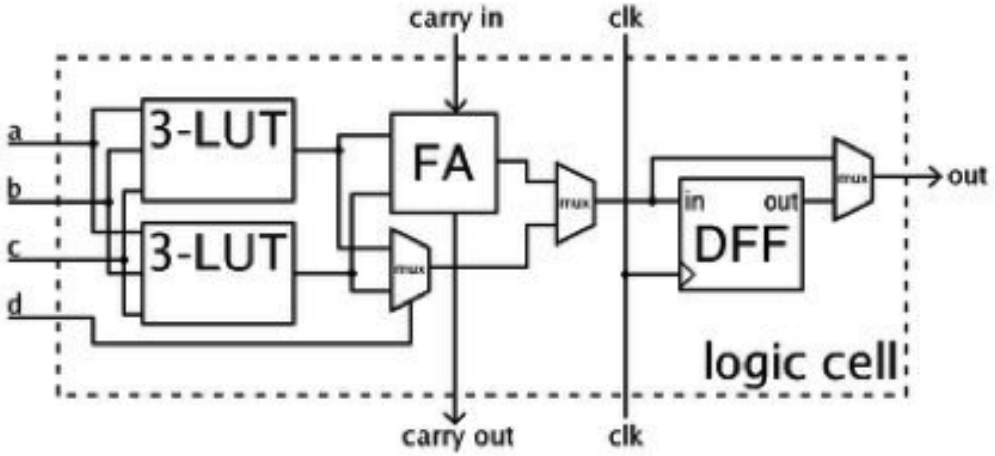
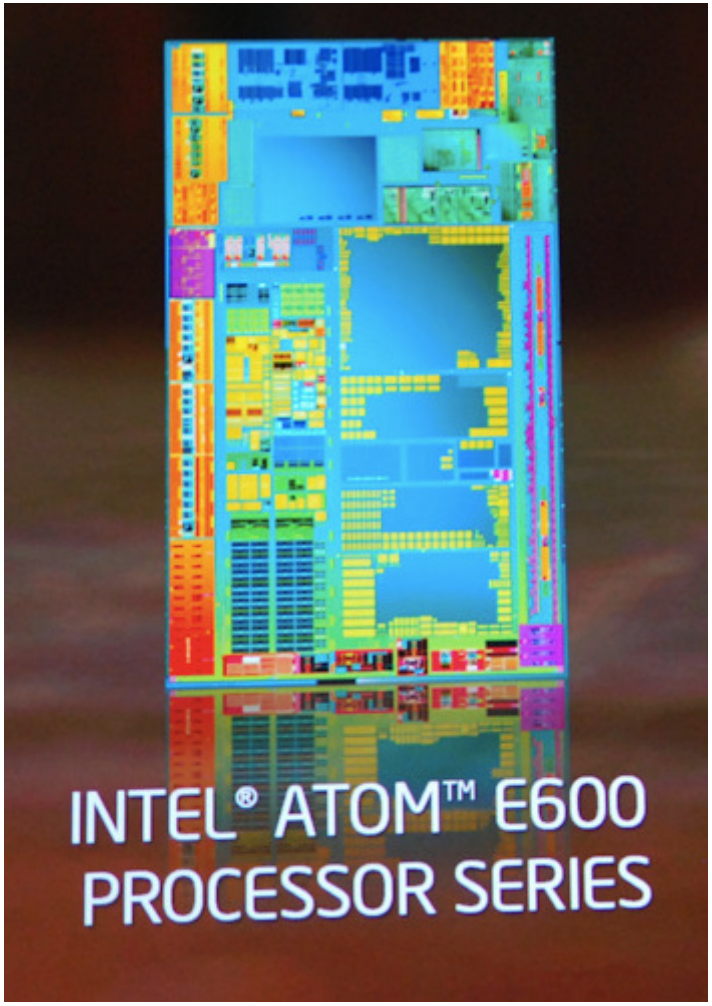


Figure 1. A Xilinx FPGA cell [1]

A Brief History of FPGAs (contd.)



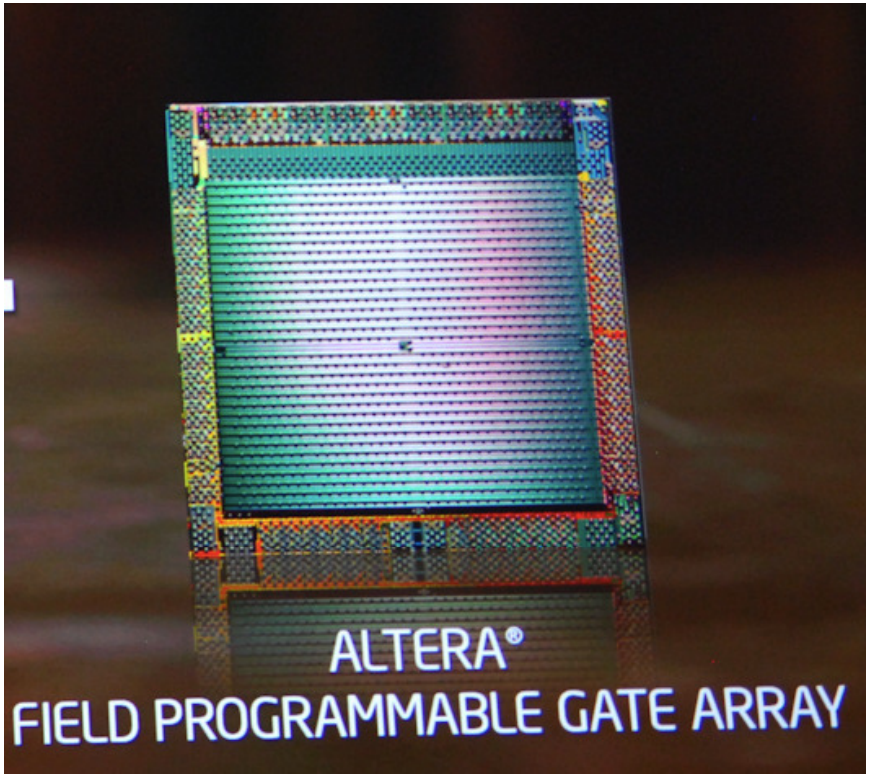
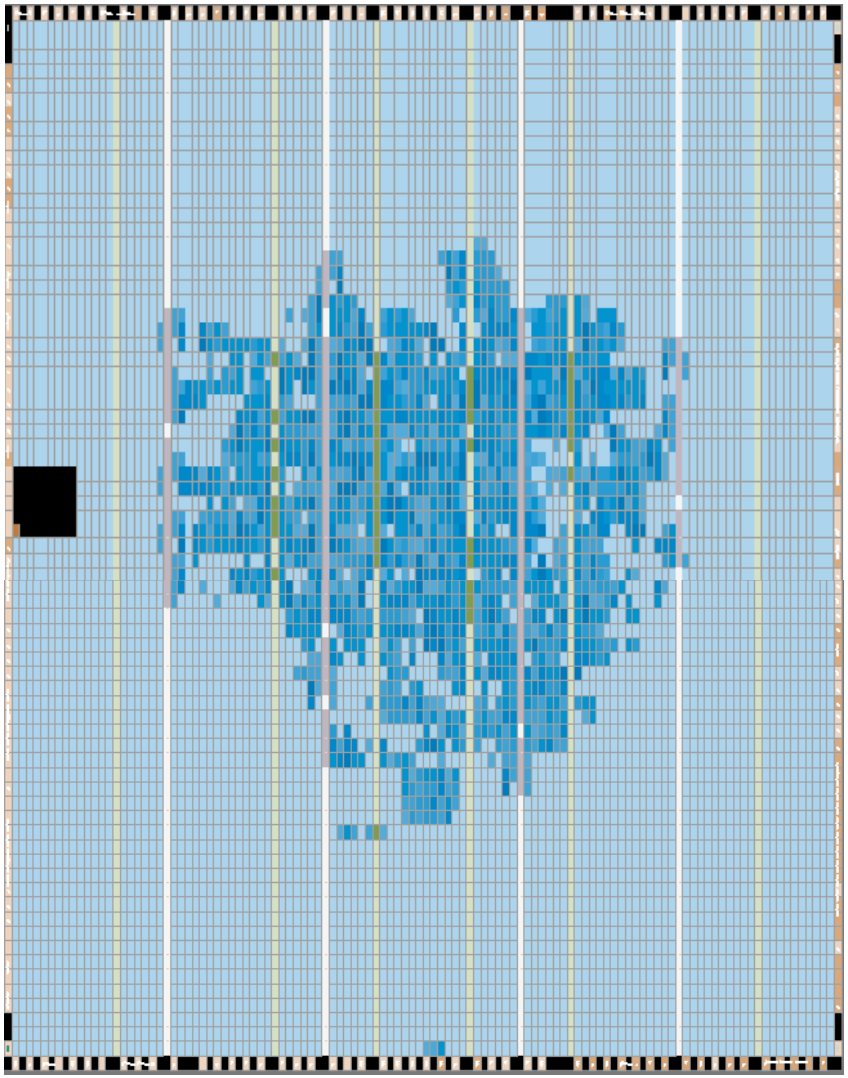
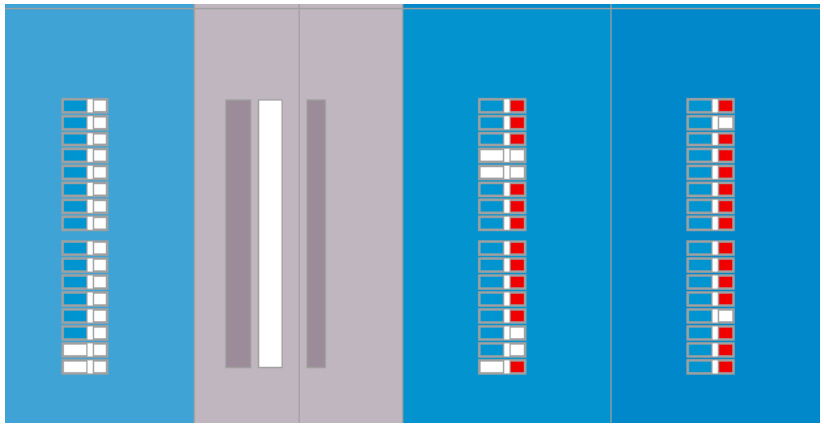


Figure 2. Processor vs. FPGA [2]

A Brief History of FPGAs (contd.)





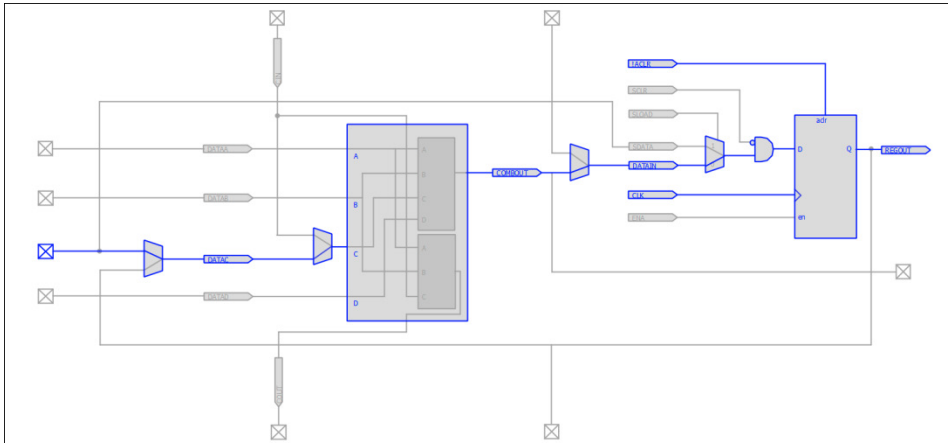


Figure 3. The Cyclone IV FPGA from Altera [1]

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Why FPGAs?

1. Unlike processors, FPGAs use dedicated hardware for processing logic [1].

2. A truly “hard” implementation of our design specification [1].

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Disadvantages of FPGAs

1. One must have a very good understanding of underlying hardware to utilize an FPGA effectively.

2. Mastering the software tools could be a steep learning curve as compared to microcontroller programming.

3. FPGA designs require timing closure by the user.

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Trend 1: ASIC and FPGA on the same die

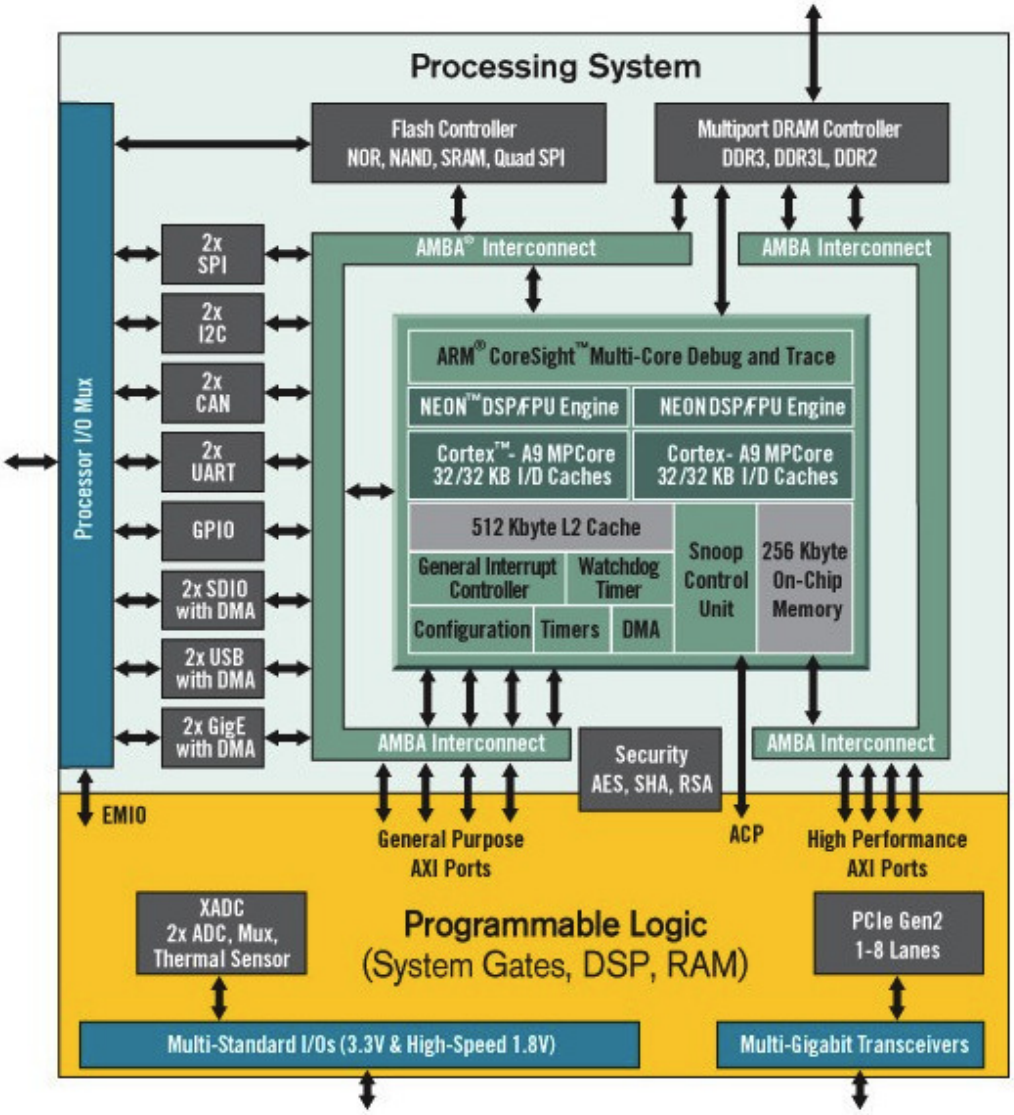

Figure 4. Zynq-7000 [4]

Trend 1: ASIC and FPGA on the same die (contd.)

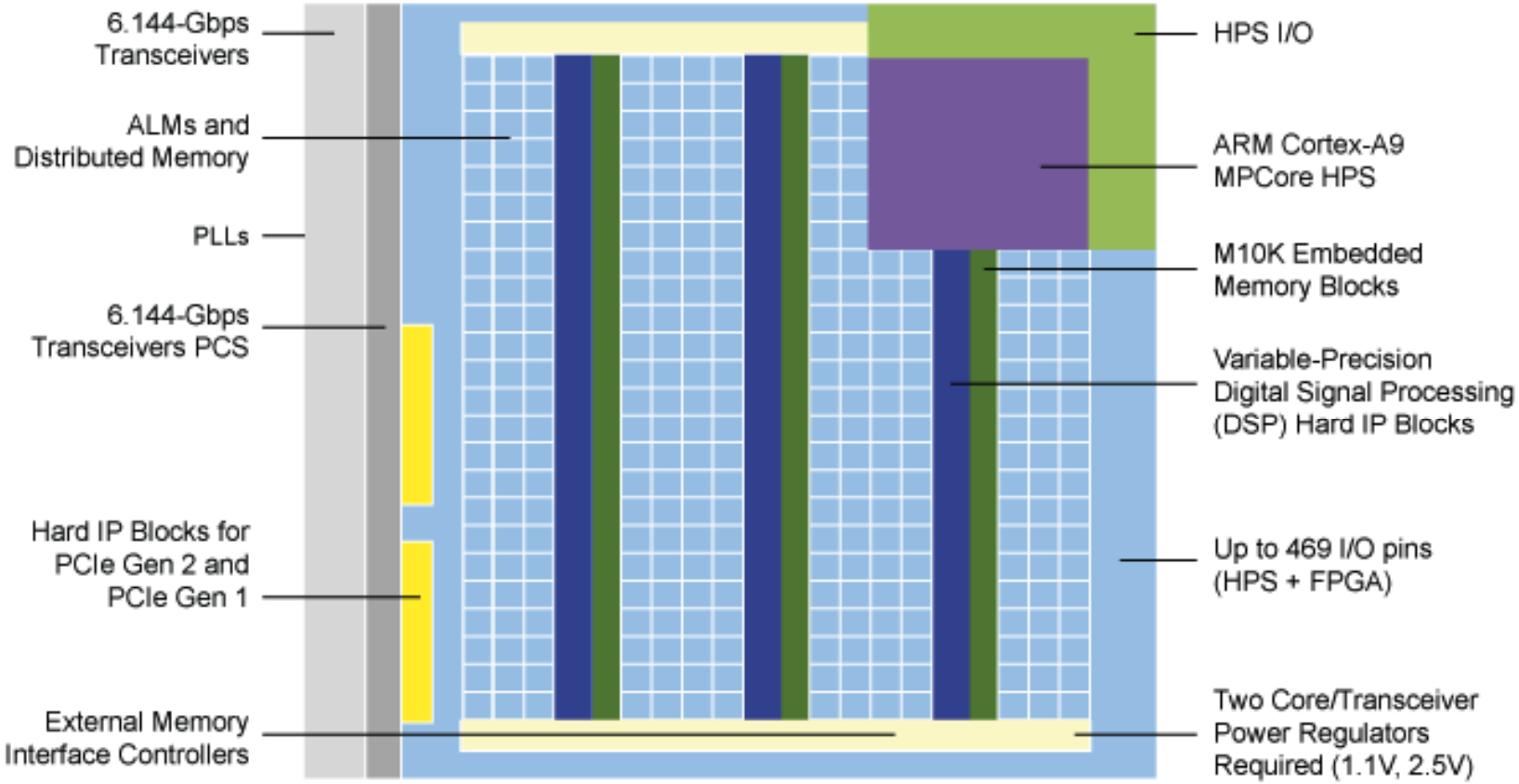

Figure 5. Cyclone V [5]

Trend 2: High (Functional) Level Design Specification: (work done jointly with VIT, thanks to Ms. Valli et. al.)

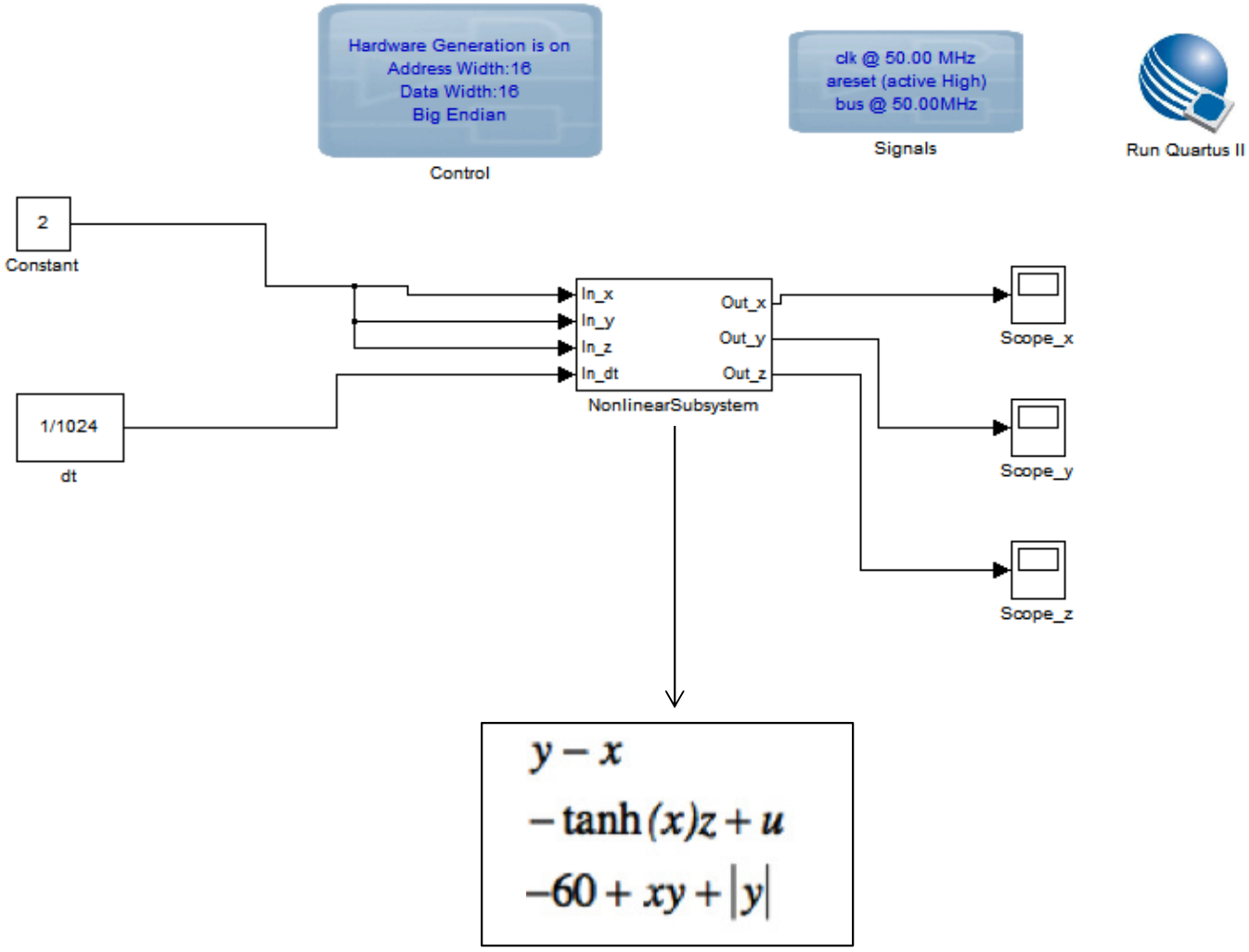

Figure 6. DSP Builder Advanced Blockset Simulink block diagram

Trend 2: High (Functional) Level Design Specification (contd.)
(work done jointly with VIT, thanks to Ms. Valli et. al.)

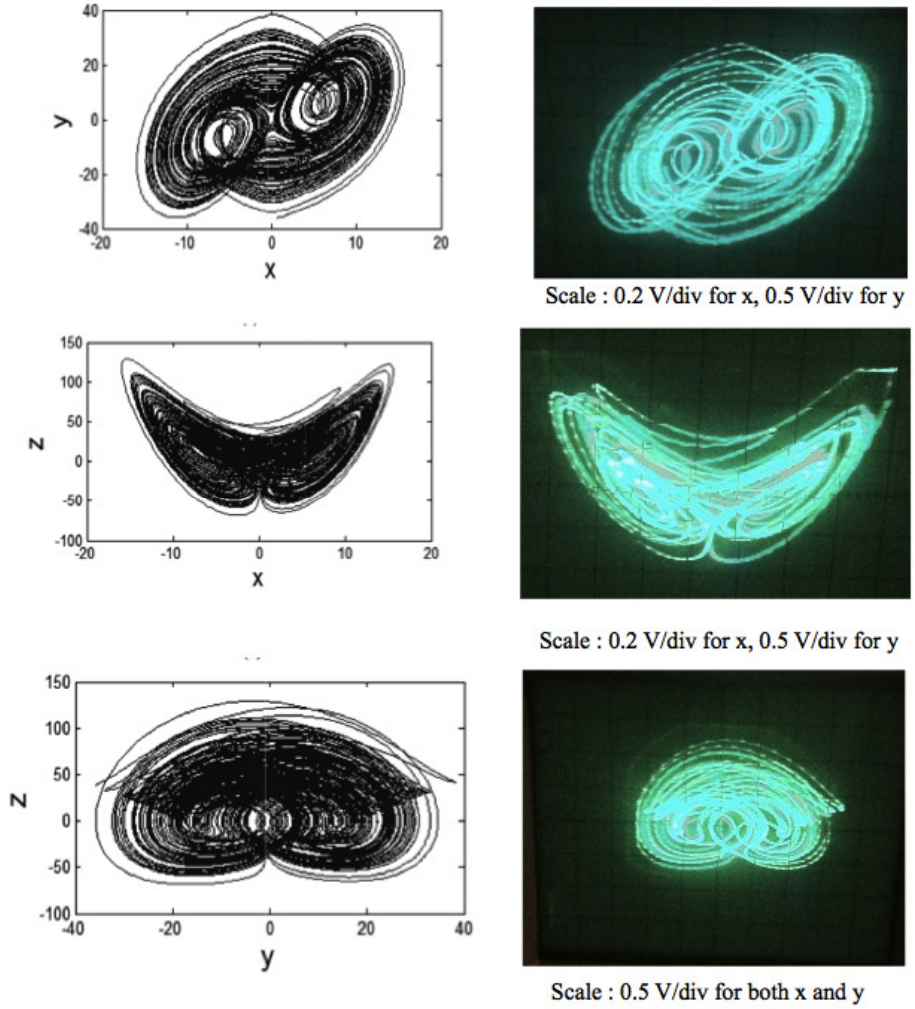

Figure 7. Simulation [6] vs. experimental results [1]

Trend 2: High (Functional) Level Design Specification (contd.)
(work done jointly with VIT, thanks to Ms. Valli et. al.)

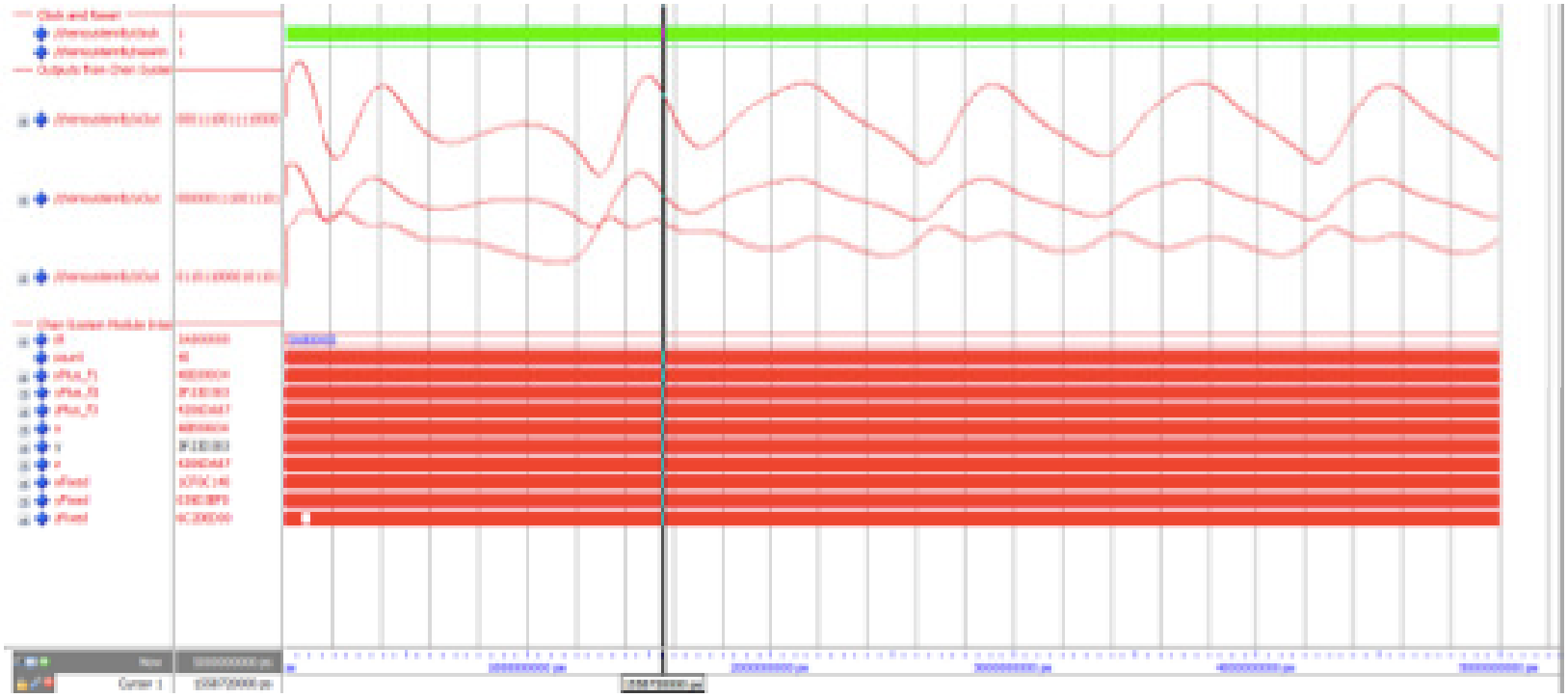

Figure 8. ModelSim Simulation

Trend 2: High (Functional) Level Design Specification (contd.)
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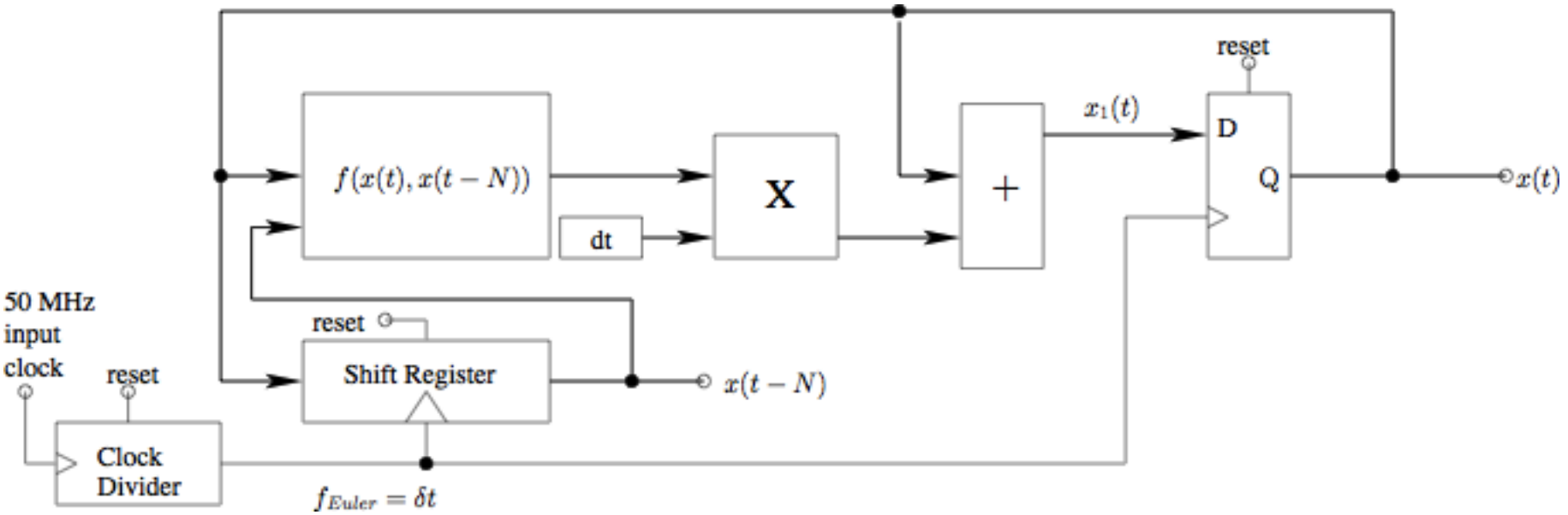

Figure 9. Implementing Delay Differential Equations.

Reference: "Synchronization in Coupled Ikeda Delay Systems – Observations using FPGAs". Valli, D. et. al., Eur. Phys. J. Special Topics. DOI: 10.1140/epjst/e2014-02144-8

Trend 2: High (Functional) Level Design Specification (contd.)
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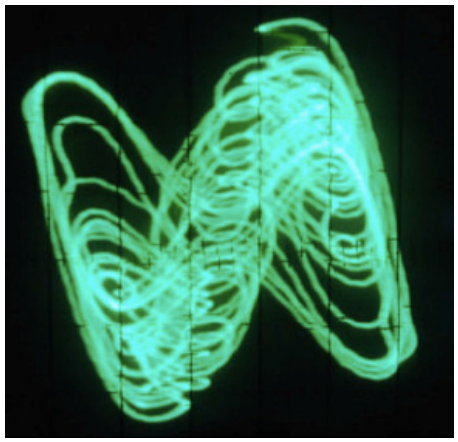
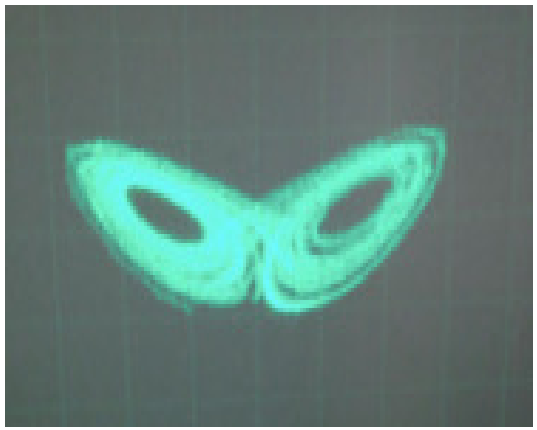


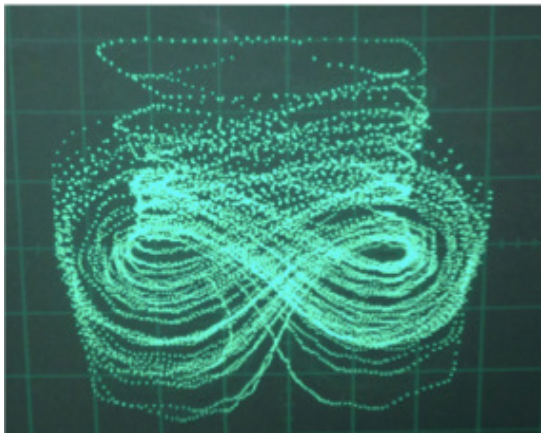
Ikeda

$$\dot{x} = \mu \sin(x(t-\tau)) - x(t)$$



Lorenz

$$\begin{aligned} \dot{x} &= \sigma(y-x) \\ \dot{y} &= -xz + \rho x - y \\ \dot{z} &= xy - \beta z \end{aligned}$$



Chen

$$\begin{aligned} \dot{x} &= a(y-x) \\ \dot{y} &= (c-a)x - xz + cy \\ \dot{z} &= xy - bz \end{aligned}$$

Figure 10. Other nonlinear dynamical (chaotic) systems

LIVE DEMO

Trend 3 : Space-Time

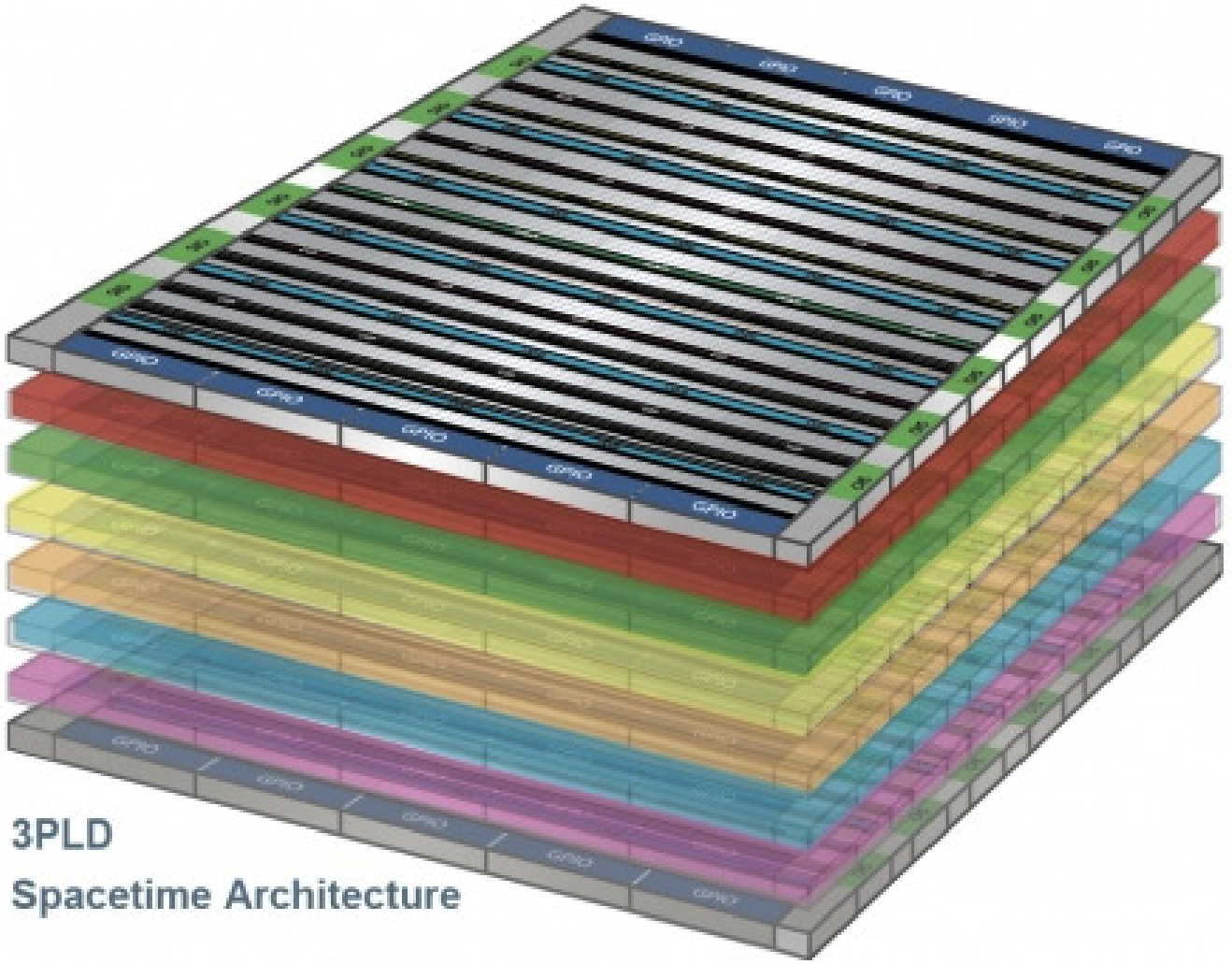


Figure 11. Tabula ABAX architecture [7].

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Conclusion

1. FPGAs are THE future of digital logic design.
2. But, for high volumes, ASICs are still preferable (although gap is closing) [3].

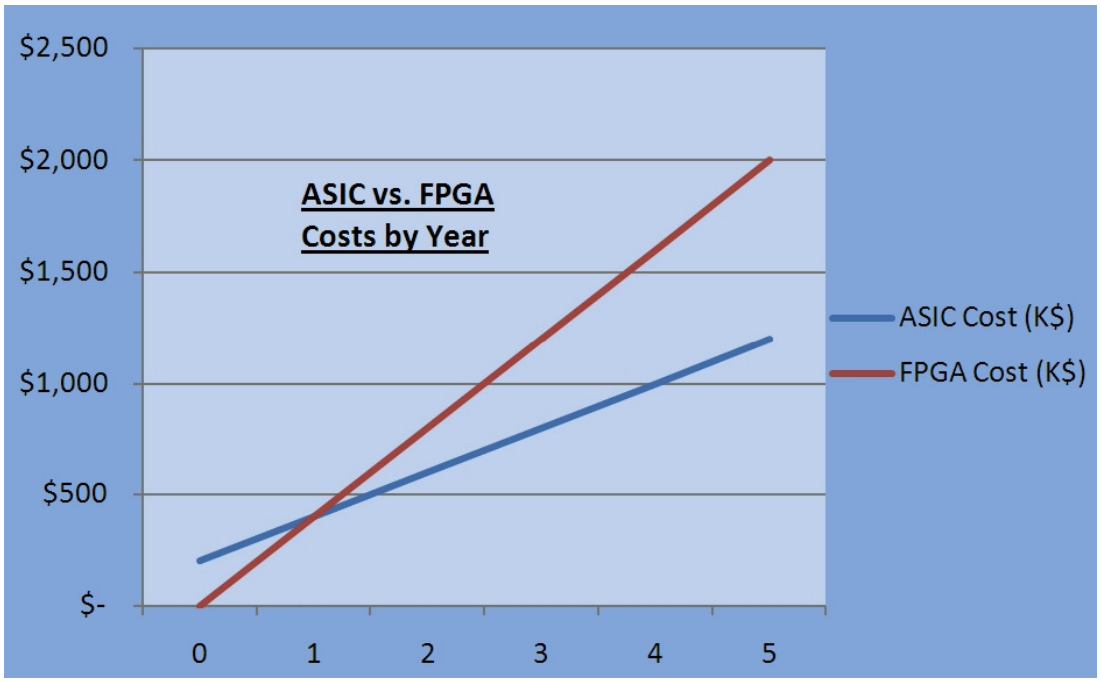

Figure 12. ASIC vs. FPGA NREs

We hope that you enjoy and learn about FPGA "programming" (**HARDWARE DESIGN**) in this workshop!

References

1. Muthuswamy, M. and Banerjee, S. "A Route to Chaos Using Integrated Circuits – The FPGA Approach". To be published by Springer in 2014.

2. Anandtech. http://images.anandtech.com/doci/3929/IDF-E600-8648.jpg Available, Online. Last accessed August 8th 2013.

3. Custom Silicon Solutions: ASICs vs FPGAs. http://blog.customsiliconsolutions.com/uncategorized/asics-vs-fpgas Available, Online. Last accessed August 8th 2013.

4. Xilinx Zynq homepage. http://www.xilinx.com/products/silicon-devices/soc/xa-zynq-7000.html Available, Online. Last accessed August 8th 2013.

5. Altera Cyclone V SOCs. http://www.altera.com/devices/processor/soc-fpga/cyclone-v-soc/cyclone-v-soc.html Available, Online. Last accessed August 8th 2013.

6. San-Um, W. and Srisuchinwong, B. "Highly Complex Chaotic System with Piecewise Linear Nonlinearity and Compound Structures". Journal of Computers, Vol. 7, No. 4, pp. 1041-1047. April 2012.

7. Tabule Space-Time White Paper. http://www.tabula.com/products/pdf/WP003.pdf Available, Online. Last accessed August 8th 2013.