



SIMPLEST CHAOTIC CIRCUIT

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A chaotic attractor has been observed with an autonomous circuit that uses only two energy-storage elements: a *linear passive* inductor and a *linear passive* capacitor. The other element is a nonlinear active memristor. Hence, the circuit has only three circuit elements in series. We discuss this circuit topology, show several attractors and illustrate local activity via the memristor's DC $v_M - i_M$ characteristic.

Keywords: Memristor; chaotic circuit; local activity.

1. Introduction

Our purpose here is to report that a chaotic attractor does exist for an autonomous circuit that has only three circuit elements: a linear passive inductor, a linear passive capacitor and a nonlinear active memristor [Chua, 1971; Chua & Kang, 1976]. Before our circuit was designed, the simplest chaotic circuit in terms of the number of circuit elements was the Four-Element Chua's circuit [Barboza & Chua, 2008]. Thus, not only does our circuit reduce the number of circuit elements required for chaos by one, it is also the *simplest* possible circuit in the sense that we also have only one *locally-active* element — the memristor. The definition of local activity [Chua, 2005] will be given later in this paper. This system is also different from Chua's circuit because we have product terms as the nonlinearity. Thus our system is more related to the Rossler [Rossler, 1976] and Lorenz [Lorenz, 1963] systems.

Nevertheless, we will show later in this paper that the memristor's characteristics could be changed to give rise to other chaotic systems.

This paper is organized as follows: we first discuss circuit topology and equations. This is followed by several plots of waveforms from the physical circuit that illustrate the period-doubling route to chaos. We then numerically compute Lyapunov exponents. Next, we plot the memristance function, DC $v_M - i_M$ characteristics of the memristor and also show the pinched hysteresis loop — the fingerprint of a memristor. The paper concludes with a discussion of future work.

2. Circuit Topology and System Equations

Consider the three-element circuit and the memristor with characteristics¹ shown in Fig. 1. The circuit

¹The memristor's internal state in Fig. 1 is given by x . This is not the same as $x(t)$ in Eq. (1). The memristor state in Eq. (1) is given by $z(t)$.

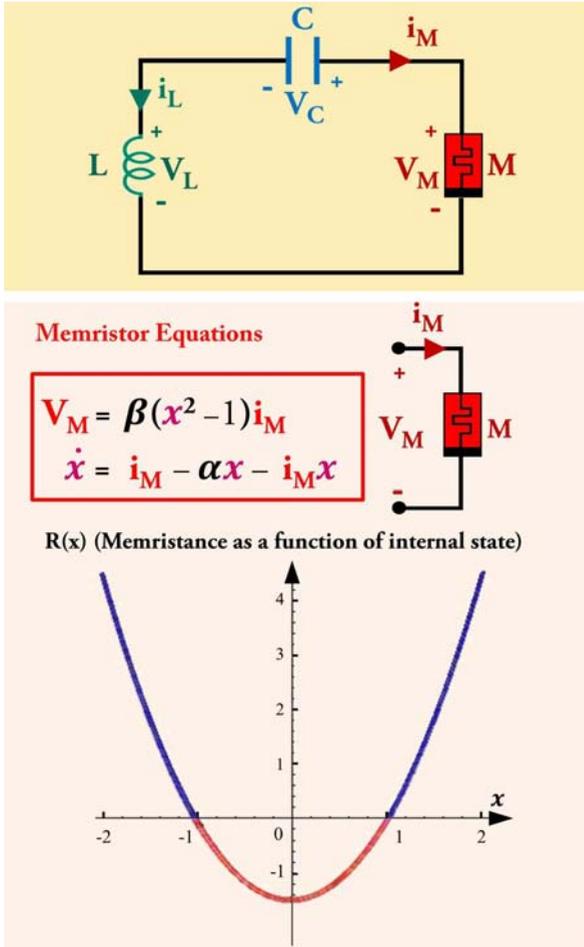


Fig. 1. The figure above shows a schematic of the proposed circuit, the two defining equations for the memristor and a plot of the memristance function $R(x) \triangleq \beta(x^2 - 1)$. The parameters are $\alpha = 0.6, \beta = 3/2, L = 3, C = 1$. Note that our memristor is a *memristive device* as defined in [Chua & Kang, 1976] and not the ideal memristor of [Chua, 1971]. We have followed the associated reference convention for each device. The region of negative memristance has also been contrasted (red) with the region of positive memristance (blue).

dynamics are described by:

$$\begin{cases} \dot{x} = y \\ \dot{y} = -\left(\frac{1}{3}\right)x + \left(\frac{1}{2}\right)y - \left(\frac{1}{2}\right)z^2y \\ \dot{z} = -y - 0.6z + yz. \end{cases} \quad (1)$$

A plot of the attractor obtained by simulating Eq. (1) (initial conditions: $x(0) = 0.1, y(0) = 0, z(0) = 0.1$) is shown in Fig. 2.

In terms of the parameters in Fig. 1, Eq. (1) becomes:

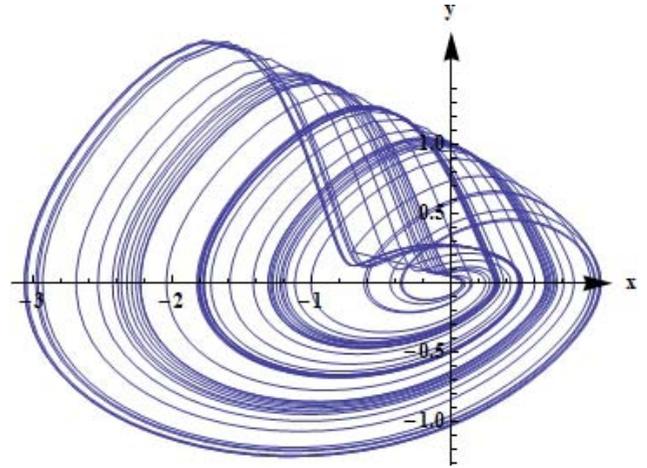


Fig. 2. The $y(t)$ versus $x(t)$ plot of the chaotic attractor from Eq. (1).

$$\begin{aligned} \dot{x} &= \frac{y}{C} \\ \dot{y} &= \frac{-1}{L}[x + \beta(z^2 - 1)y] \\ \dot{z} &= -y - \alpha z + yz. \end{aligned} \quad (2)$$

The parameter values are $C = 1, L = 3, \beta = 3/2 = 1.5, \alpha = 0.6$. A derivation of Eq. (2) is given in Appendix A. The state variables in terms of circuit variables are $x(t) \triangleq v_C(t)$ (voltage across capacitor C), $y(t) \triangleq i_L(t)$ (current through inductor L) and $z(t)$ is the internal state of our memristive system, as defined in Fig. 1. Notice that we are using the more general *memristive system* [Chua & Kang, 1976] model in Eq. (2), defined below:

$$v_M = R(x)i_M \quad (3)$$

$$\dot{x} = f(x, i_M) \quad (4)$$

where $f(x, i_M)$ is the *internal state* function of the memristor, $R(x)$ is the *memristance*. The characteristics of our memristor are described in Fig. 1.

It is easy to understand why we resorted to the more general *memristive system*. From basic circuit theory, it is not possible to have a single loop circuit with three independent state variables if we use the ideal *charge-controlled*² memristor. This can be easily seen if we recall the definition of a charge-controlled memristor [Chua, 1971] as:

$$v_M = M(q)i_M \quad (5)$$

$$\dot{q} = i_M. \quad (6)$$

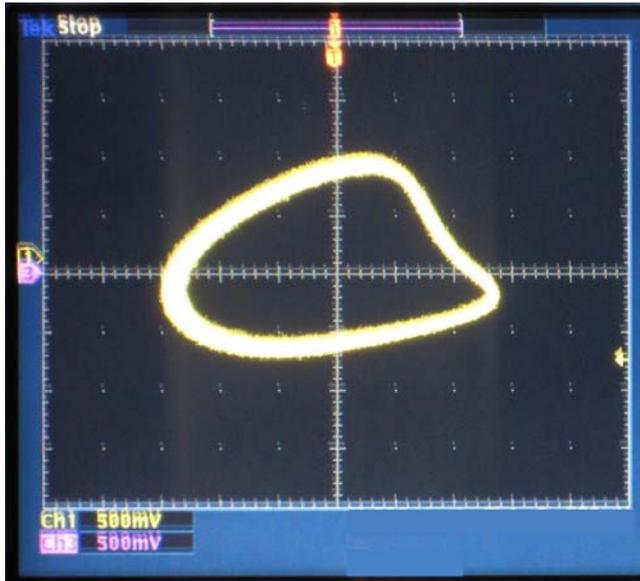
²Analogous arguments apply for a *flux-controlled* memristor.

In a single loop circuit there is only one current flowing through all elements by Kirchhoff's Current Law [Chua, 1969] and all the voltages are linearly-related by Kirchhoff's Voltage Law [Chua, 1969]. Hence the internal state of a charge-controlled memristor does not give rise to a third state variable. Since the Poincaré–Bendixson theorem implies that we need three state variables for an autonomous

continuous-time system to be chaotic [Bendixson, 1901], we use the more general *memristive system* as our third circuit element.

3. Results from the Physical Circuit

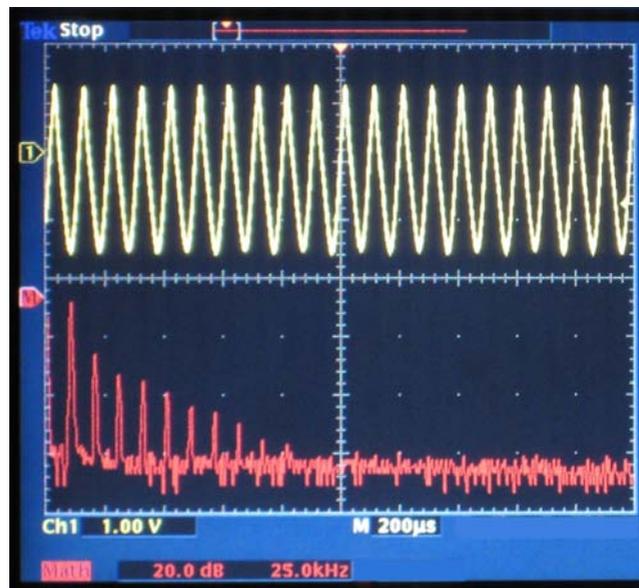
The physical circuit realization of our system is shown in Appendix B, Fig. 11. Note from the



(a)



(b)

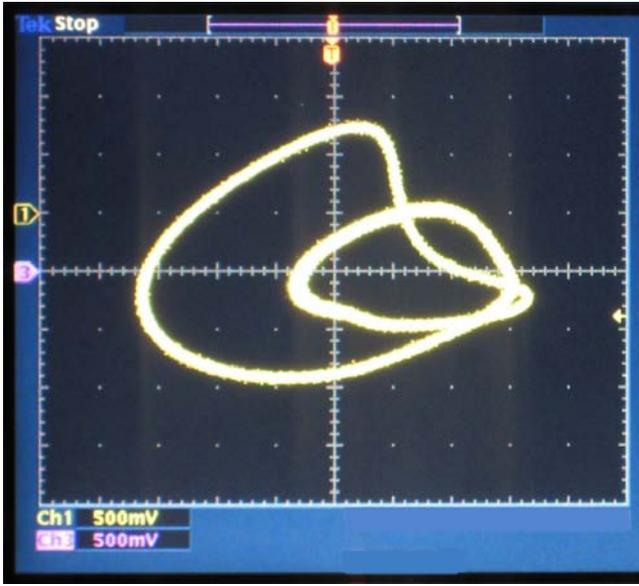


(c)

Fig. 3. Plots of Period-One Limit Cycle: (a) Phase plot ($i_L(t)$ versus $v_C(t)$); (b) Time domain waveforms ($v_C(t)$ is Channel 1, $i_L(t)$ is Channel 3) and (c) Fast Fourier Transform of $v_C(t)$ from our circuit. The scales along the axes are: (a) 0.5 V/division on each axis; (b) 1.00 V/division for Channels 1 and 3, 200 μ s/division for the time axis; (c) 1.00 V/division for Channel 1, 200 μ s/division for the time axis, 20.0 dB/division and a 25.0 kHz center frequency for the Fast Fourier Transform plot. $\beta \approx 1.2$.

schematic that our realization is *not* an analog computer, where each component has an associated nonzero current and voltage whose product is power. Also, due to restrictions imposed by component values, the parameters in Eq. (2) corresponding with the physical system are $C = 1$, $L = 3.3$, $\beta = 1.7$, $\alpha = 0.2$.

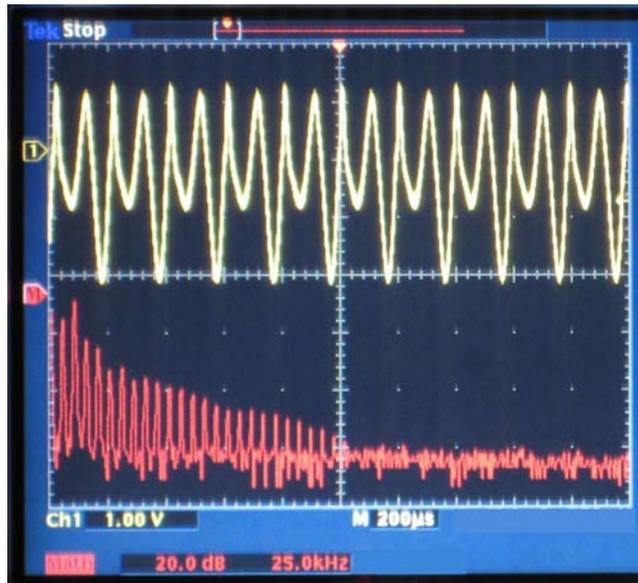
Figures 3–5 show results from the physical circuit. We have plotted state variable $x(t)$ ($v_C(t)$, voltage across the capacitor) on the x -axis and $y(t)$ ($i_L(t)$, current through the inductor) on the y -axis. The figures illustrate period-doubling route to chaos. The bifurcation parameter from Eq. (2) is β .



(a)



(b)

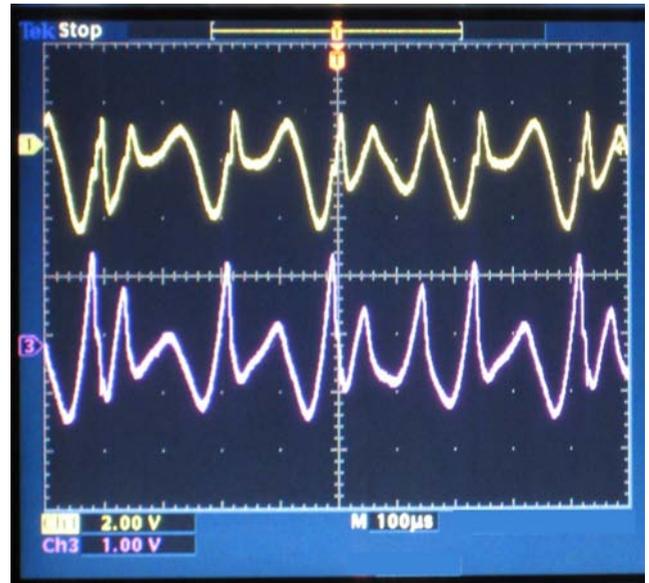


(c)

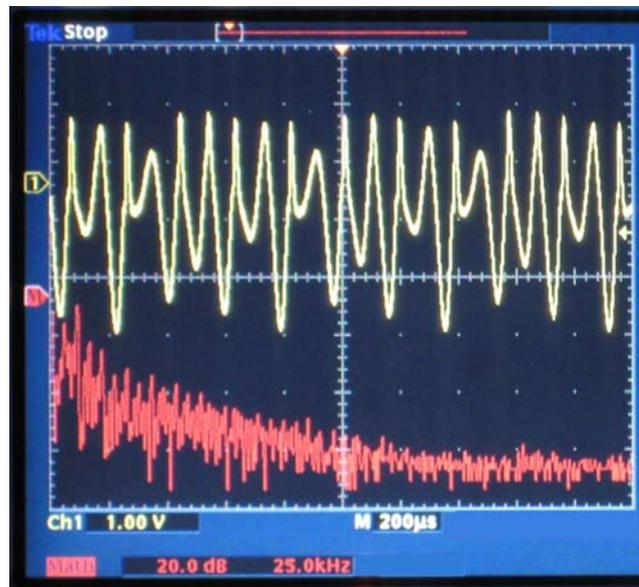
Fig. 4. Plots of Period-Two Limit Cycle: (a) Phase plot ($i_L(t)$ versus $v_C(t)$); (b) Time domain waveforms ($v_C(t)$ is Channel 1, $i_L(t)$ is Channel 3) and (c) Fast Fourier Transform of $v_C(t)$ from our circuit. The scales along the axes are: (a) 0.5 V/division on each axis; (b) 1.00 V/division for Channels 1 and Channel 3, 100 μ s/division for the time axis; (c) 1.00 V/division for Channel 1, 200 μ s/division for the time axis, 20.0 dB/division and a 25.0 kHz center frequency for the Fast Fourier Transform plot. $\beta \approx 1.3$.



(a)



(b)



(c)

Fig. 5. Plots of (a) Chaotic attractor ($i_L(t)$ versus $v_C(t)$); (b) Time domain waveforms ($v_C(t)$ is Channel 1, $i_L(t)$ is Channel 3) and (c) Fast Fourier Transform of $v_C(t)$ from our circuit. The scales along the axes are: (a) 0.5 V/division on each axis; (b) 2.00 V/division for Channel 1, 1.00 V/division for Channel 3, 100 μs /division for the time axis; (c) 1.00 V/division for Channel 1, 200 μs /division for the time axis, 20.0 dB/division and a 25.0 kHz center frequency for the Fast Fourier Transform plot. $\beta \approx 1.7$.

With $\beta \approx 1.2$ we obtain Fig. 3. Both the phase plot and the time domain waveforms indicate a periodic limit-cycle. This is empirically confirmed by the Fast Fourier Transform (FFT) from the scope, the sharp peaks clearly show the harmonics.

Increasing β to approximately 1.3 gives us Fig. 4. The period-doubling route to chaos can be empirically confirmed by comparing Figs. 4(c) to 3(c). The FFT in Fig. 4(c) shows a second subset of harmonics as compared to Fig. 3(c).

$\beta \approx 1.7$ gives us chaos. Notice the wideband nature of the spectra in Fig. 5(c).

3.1. Comparison between physical and theoretical attractors

In Fig. 6, we plot two attractors that were measured from the circuit and compare them to the results from a Mathematica simulation.

4. Numerical Evidence of Chaos: Lyapunov Exponents

Lyapunov exponents provide empirical evidence of chaotic behavior. They characterize the rate of separation of infinitesimally close trajectories in state-space [Eckmann & Ruelle, 1985; Wolf *et al.*, 1985]. The rate of separation can be different for different orientations of the initial separation vector, hence

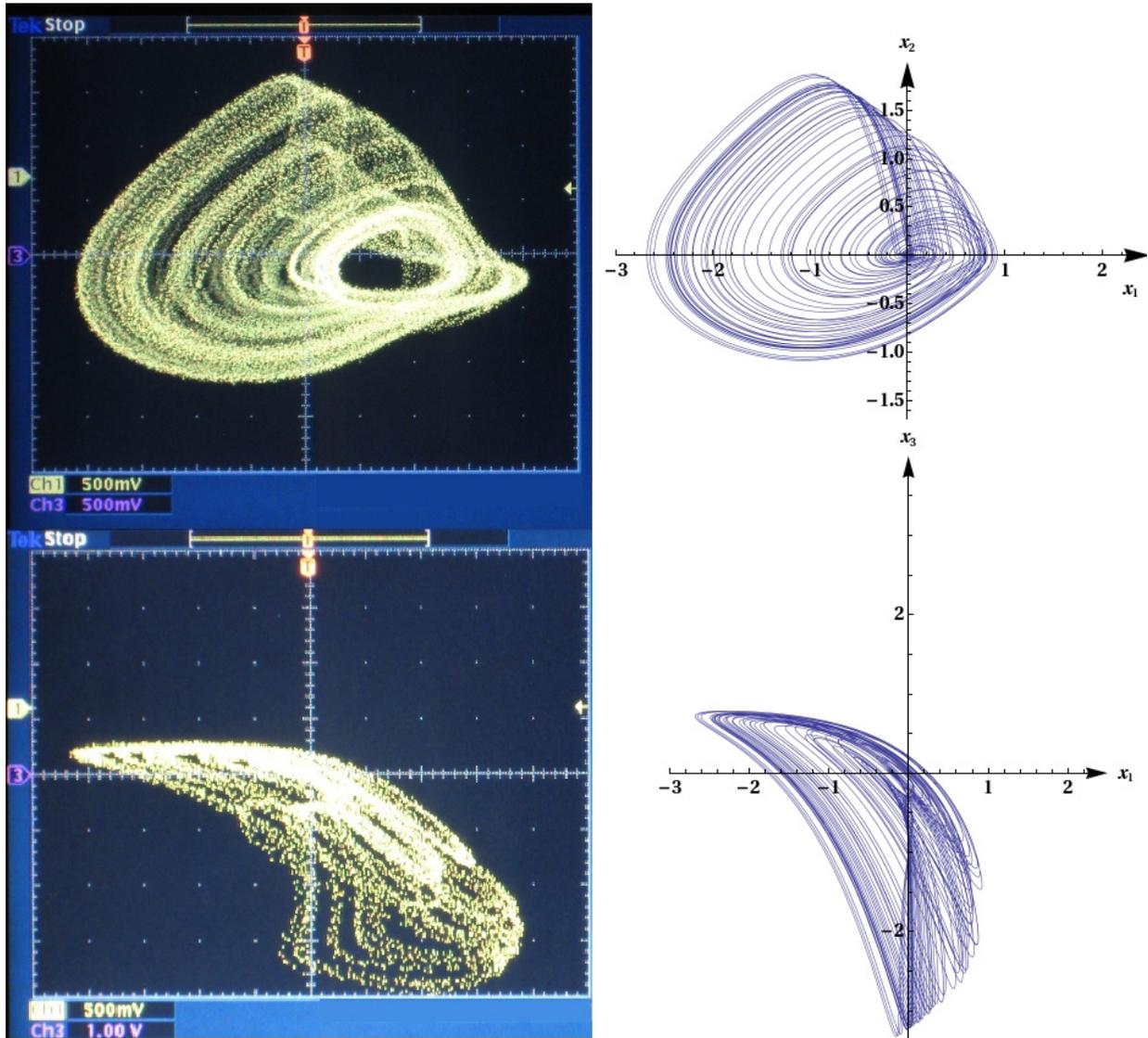


Fig. 6. In this figure, we compare experimental versus theoretical attractors. The top two sets of attractor plots $y(t)$ ($i_L(t)$, current through the inductor) versus $x(t)$ ($v_C(t)$, voltage across the capacitor). The axes scales for the experimental attractor on the top-left are 0.5 V/division. Hence for the experimental attractor, the $x(t)$ values range from -2.0 V to 2.0 V. The $y(t)$ values range from -1.0 V to 1.5 V. For the theoretical attractor on the top-right, the $x(t)$ values range from ≈ -2.75 to ≈ 1.0 . The $y(t)$ values for the theoretical attractor range from -1.0 to approximately 1.7 . Hence, the $x(t)$ values for the two attractors are offset. This is because the origin $(0,0)$ for the experimental attractor has been shifted to the right for clarity on the oscilloscope. The bottom two sets of attractors plot $z(t)$ (internal memristor state) versus $x(t)$ ($v_C(t)$, voltage across the capacitor). The axes scales for the experimental plot are 0.5 V/division for the horizontal and 1.00 V/division for the vertical axes. For the theoretical plot, the $x(t)$ values range from -2.5 to 1.0 . The $y(t)$ values range from approximately -3 to 0.5 . The bottom experimental attractor shows some distortion when $z(t)$ is close to -3.0 V.

Table 1. Comparison of Lyapunov exponents from different methods.

β Value	Time Series Method	QR Method
1.2	0, -0.003, -0.429	0, -0.004, -0.433
1.3	0, -0.012, -0.418	0, -0.014, -0.424
1.7	0.029, 0, -0.47	0.035, 0, -0.48

the number of Lyapunov exponents is equal to the number of dimensions in phase space. So for a three-dimensional autonomous continuous time system, we will have three Lyapunov exponents.

A positive Lyapunov exponent implies an expanding direction in phase space. However, if the *sum* of Lyapunov exponents is negative, then we have contracting volumes in phase space. These two seemingly contradictory properties are indications of chaotic behavior in a dynamical system. If two exponents are negative and the other exponent is zero, this indicates that we have a limit cycle [Wolf, 1986]. The values of the Lyapunov exponents computed using two different methods (the time-series method [Govorukhin, 2008] and the QR method [Siu, 2008]) are summarized in Table 1.

Notice that for $\beta = 1.7$, we have one positive Lyapunov exponent and the sum of the Lyapunov exponents is negative indicating chaotic behavior.

5. Memristor Characteristics

In this section, we illustrate several experimental and theoretical characteristics of the proposed memristor.

5.1. Memristance function $R(x)$

Recall that the memristance function is defined as $R(x) \triangleq \beta(x^2 - 1)$. A plot of experimental and theoretical $R(x)$ is shown in Fig. 7. We used $\beta = 1.7$. Details on experimentally plotting the memristance curve are given in Appendix C.

5.2. DC $v_M - i_M$ characteristics

Figure 8 compares the experimental and theoretical DC $v_M - i_M$ characteristics of the memristor. We have plotted several (i_M, v_M) data points in a $100 \mu s$ interval from the physical circuit on the theoretical $v_M - i_M$ curve. Notice that most of the points lie in the negative resistance or *locally-active* region. The significance of negative resistance region and details on experimentally obtaining this curve are given in Appendix D.

5.3. Pinched hysteresis loop

Figure 9 shows two pinched hysteresis loops, one at low frequency and the other at high frequency.

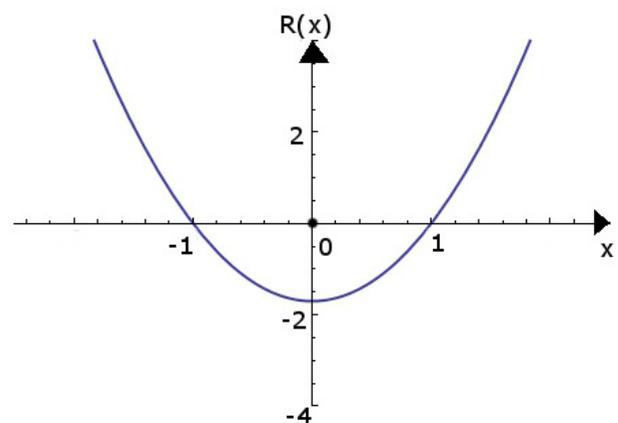
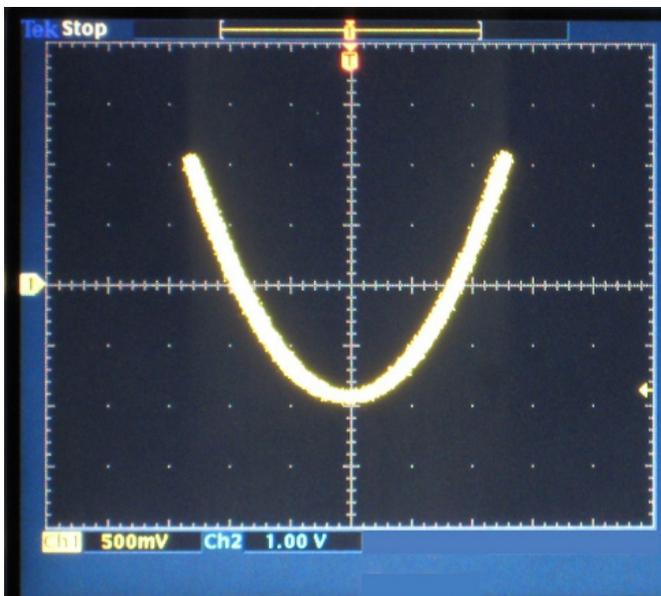


Fig. 7. Plots of experimental memristance (left) and theoretical memristance (right). For the experimental $R(x)$, horizontal axis scale is 0.5 V/division; vertical axis scale is 1.00 V/division. We plot $x(t)$ on the horizontal, v_M on the vertical. With a 1 V division on the vertical scale, the experimental curve crosses the vertical axis at ≈ -1.8 V. The theoretical plot crosses the vertical axis at -1.7 . The horizontal axis crossing for the experimental curve is at -1 V and approximately 0.9 V. For the theoretical curve, it occurs at $x = \pm 1$.

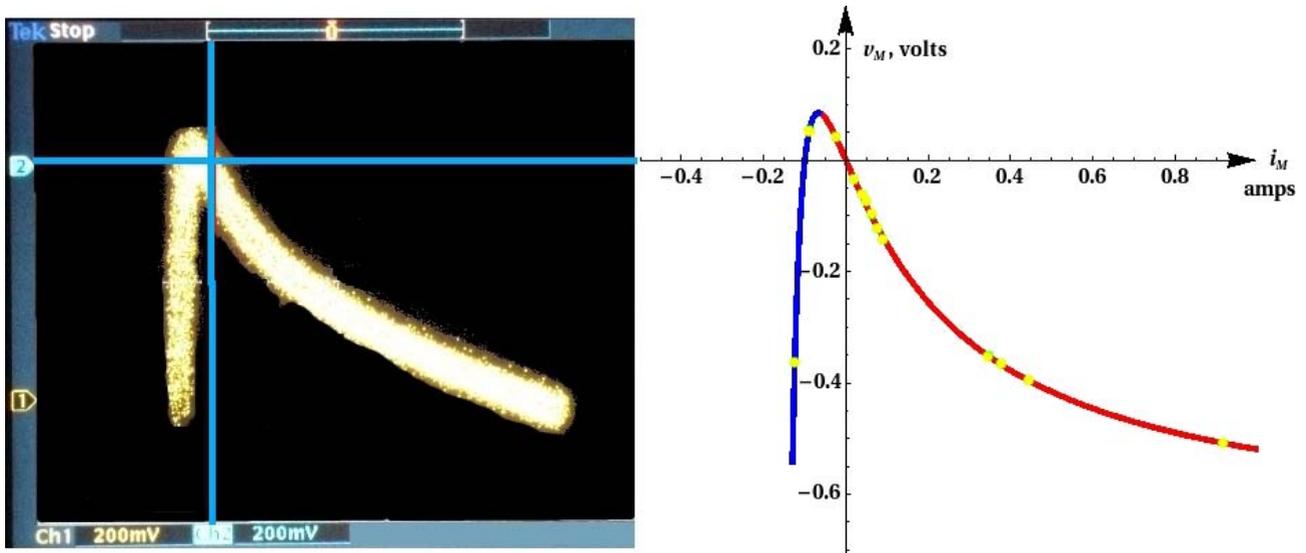


Fig. 8. Plots of experimental DC curve (left) and theoretical DC curve (right). Experimental plot axes scales are 0.2 V/division. The experimental oscilloscope picture has been offset for clarity, we have marked the axes in blue. v_M is on the vertical axis, i_M on the horizontal axis. We have also plotted several experimental (i_M, v_M) points from the chaotic waveforms on the theoretical DC curve. Notice that most points lie in the *locally-active* region.

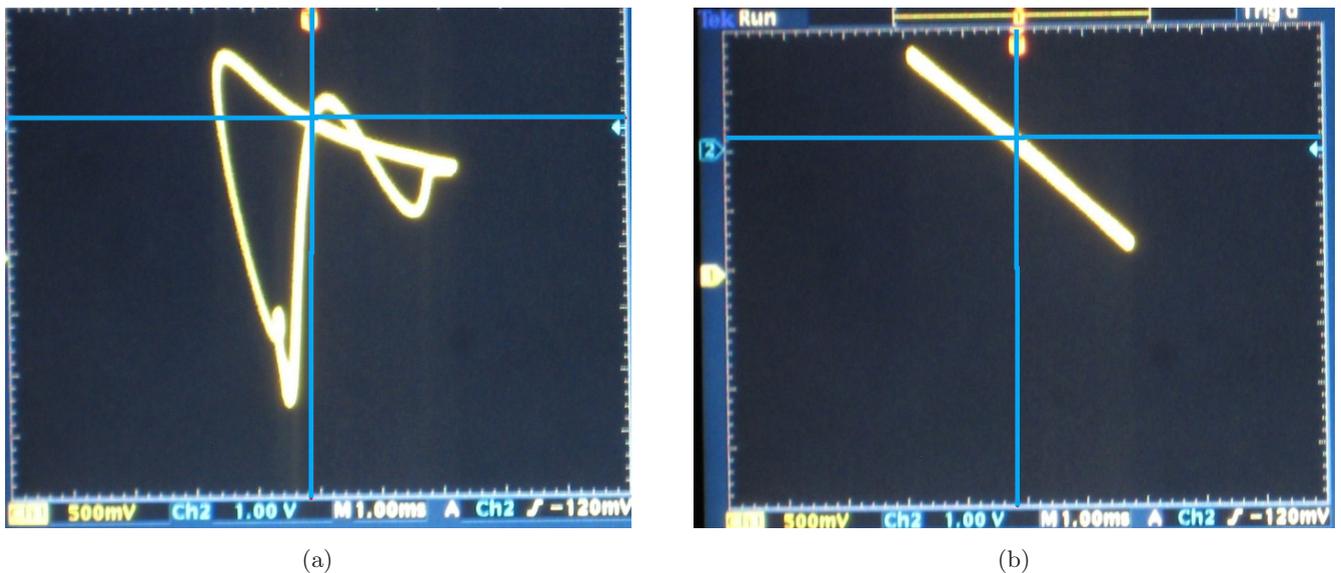


Fig. 9. Memristor pinched hysteresis loop (Lissajous figures). (a) Pinched hysteresis loop, 3 kHz. (b) Pinched hysteresis loop, 35 kHz. Axes scales for (a) and (b) are 0.5 V/division for the x -axis and 1.00 V/division for the y -axis. Vertical axis is v_M , horizontal axis is i_M .

The test circuit for obtaining the pinched hysteresis loop is given in Fig. 14 in Appendix D (the same circuit for obtaining the memristor’s DC $v_M - i_M$ characteristics). Notice that the pinched hysteresis loop in Fig. 9(a) degenerates into a *linear time-invariant resistor* in Fig. 9(b) as we increase the frequency. This indicates that the underlying memristive system is *BIBO* (bounded-input

bounded-output) stable [Chua & Kang, 1976]. More on this will be said in the conclusion.

6. Conclusions and Future Work

In this work, we reported the existence of an autonomous chaotic circuit that utilizes only three elements in series. We have shown attractors from

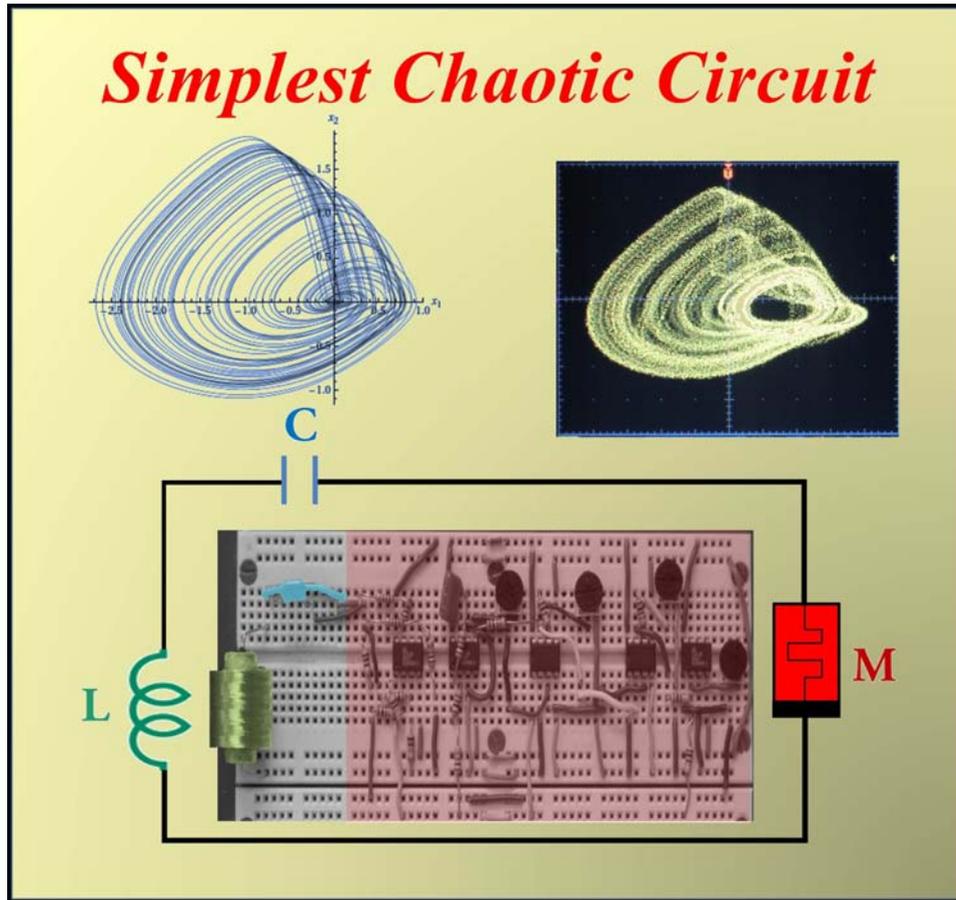


Fig. 10. The simplest chaotic circuit with only three circuit elements in series — the inductor, capacitor and a memristor. The memristor is the only active nonlinear device. It requires ± 15 V DC power supplies (not shown for clarity). The other two circuit elements — inductor and capacitor — are highlighted. We also plot the theoretical attractor and the chaotic attractor obtained from the physical implementation.

this circuit along with an illustration of period-doubling route to chaos. Figure 10 summarizes our circuit. Note that the memristor plays two roles: the third essential state variable and the essential nonlinearity.

An interesting future direction would be to further investigate the system from Eq. (2). If we use the general definition of a memristive system [Chua & Kang, 1976], Eq. (2) becomes:

$$\begin{aligned} \dot{x} &= \frac{y}{C} \\ \dot{y} &= \frac{-1}{L}(x + R(z)y) \\ \dot{z} &= f(z, y). \end{aligned} \quad (7)$$

In Eq. (7), we are free to pick $R(z)$ and $f(z, y)$. This paper has illustrated one particular choice. There are other potential choices for $R(z)$ and $f(z, y)$. One of our initial choices was $R(z) = -z$ and

$f(z, y) = f(y) = 1 - y^2$. This leads to:

$$\begin{aligned} \dot{x} &= \frac{y}{C} \\ \dot{y} &= \frac{-1}{L}(x - zy) \\ \dot{z} &= 1 - y^2. \end{aligned} \quad (8)$$

We realized that the system above has already been proposed in [Sprott, 1994]. If $L = C = 1$, Eq. (8) is case A in [Sprott, 1994]. But with this choice of $R(z)$ and $f(y)$, the associated memristive system is *not BIBO (bounded-input bounded-output) stable*. For a proof of BIBO instability, refer to Appendix E. In other words, we cannot obtain a pinched hysteresis loop to characterize the memristor. Hence imposing a practical constraint for the memristive system to be BIBO stable, we could ask the question: does there exist a three-element chaotic circuit that is *canonical* [Chua, 1993] like Chua's circuit?

It would also be very useful if the BIBO stability of our proposed memristive system is theoretically investigated. Another avenue of investigation is to improve the memristor emulator. Eliminating the sensing resistor using the technique proposed in [Persin & Di Ventra, 2009b] is a good topic for future work.

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Appendix

A. Derivation of Circuit Equations

Recall that we have $x(t) \triangleq v_C(t)$ (voltage across capacitor C), $y(t) \triangleq i_L(t)$ (current through inductor L) and $z(t)$ is defined as the internal state of our memristive system. From the constitutive relation of a linear capacitor [Chua, 1969], we have the following equation from Fig. 1:

$$\frac{dv_C}{dt} = \frac{i_L}{C} \quad (\text{A.1})$$

Using our circuit variable to state variable mappings, we get our first state equation:

$$\boxed{\dot{x} = \frac{y}{C}} \quad (\text{A.2})$$

Applying Kirchhoff's Voltage Law around the loop [Chua, 1969] in Fig. 1 and simplifying using the constitutive relations of the inductor, capacitor and memristor, we get

$$\begin{aligned} v_L + v_C &= v_M \\ \Rightarrow L \frac{di_L}{dt} &= -v_C + v_M \\ \Rightarrow \frac{di_L}{dt} &= \frac{1}{L}(-v_C + v_M) \\ &= \frac{1}{L}(-v_C + \beta(z^2 - 1)i_M) \\ &= \frac{1}{L}(-v_C + \beta(z^2 - 1)(-i_L)) \\ \Rightarrow \frac{di_L}{dt} &= \frac{-1}{L}(v_C + \beta(z^2 - 1)i_L) \end{aligned} \quad (\text{A.3})$$

Hence in terms of state variables, we have obtained our second state-equation:

$$\boxed{\dot{y} = \frac{-1}{L}(x + R(z)y)} \quad (\text{A.4})$$

Note that $R(z) \triangleq \beta(z^2 - 1)$. Finally, we define the differential equation governing the internal state of our memristor to be:

$$\boxed{\dot{z} \triangleq -y - \alpha z + yz} \quad (\text{A.5})$$

B. Detailed Circuit Schematic

In this appendix we will derive the system equations for the circuit shown in Fig. 11. In the circuit, we

have highlighted three energy storage elements in color, to correspond to Fig. 1. Notice that the internal state of the memristor is thus stored in capacitor C_f . The entire memristor analog emulator (enclosed in a red box) is an *active nonlinear* element, powered by ± 15 V DC power supplies.

Throughout this appendix please refer to Fig. 11 for part numbers and component labels. All resistors used are standard 10% tolerance. Potentiometers are standard linear type. A 5% tolerance inductor is used along with 10% tolerance ceramic disc capacitors. The AD633 multipliers are used because of their wide bandwidth. The AD712 is a low cost BiFET input op-amp. We also used a 4.7 nF power supply filter capacitor between ± 15 V and ground.

Note that we have used the standard passive sign convention for all currents and voltages.

B.1. Realizing the first state equation

Using the constitutive relationship of the capacitor C_n we get:

$$\boxed{\frac{dv_C}{dt} = \frac{i_L}{C_n}} \quad (\text{B.1})$$

B.2. Sensing the current

The concept behind realizing a memristor is to first sense the current flowing through the circuit by using sensing resistor R_s . In our case, we have $R_s = 100 \Omega$ connected to the difference amplifier U3B. Hence, the output of U3B is:

$$v_O = \frac{R_{s1}}{R_{s2}} 100 i_M = 10\,000(-i_L) = -I_s i_L \quad (\text{B.2})$$

Hence, we now have a current scaled by a factor of I_s and mapped into voltage v_O . The significance of this scaling factor will become apparent later in this appendix.

B.3. Realizing memristor function $R(x)$

Op-amp U3A and multipliers U4, U5 are used to implement the memristance function $R(x)$. Using the datasheets of the multipliers [Analog, 2010] and the connections shown in the schematic, we can see that the output of multiplier U5 is $-x^2 v_O$. We use the resistive divider (resistors R_1 , $R_{10 \text{ kpot}}$, $R_{1,2}$,

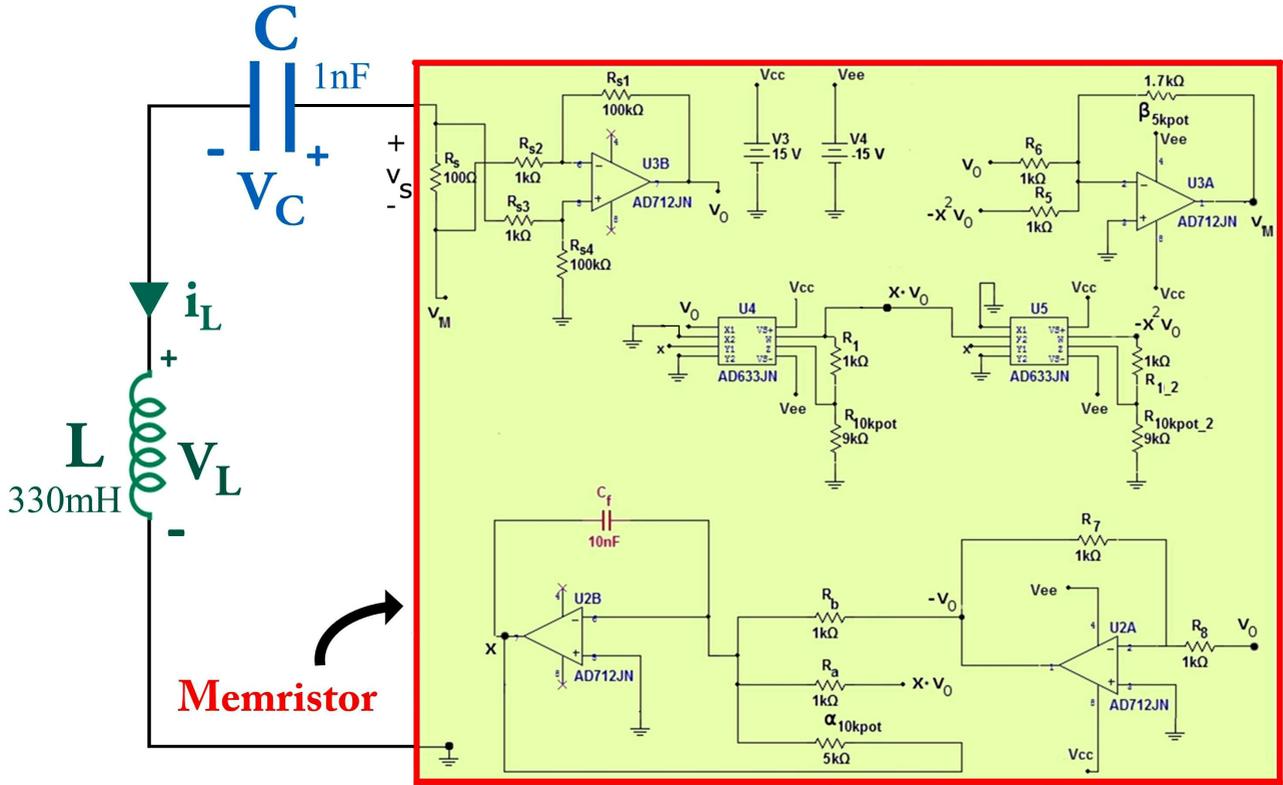


Fig. 11. Schematic of the three-element memristor-based chaotic circuit. Note that in the appendix, we have used C_n and L_n instead of C and L respectively. This notation distinguishes realistic capacitor and inductor values from the theoretical numbers.

$R_{10\text{kpot}_2}$) between pins W and Z in the two multipliers to cancel the multiplier internal scaling factor of 10. Op-amp U3A is an inverting summing amplifier. The output v_M is given by:

$$v_M = -\frac{\beta_{5\text{kpot}}}{R_6} v_O - \frac{\beta_{5\text{kpot}}}{R_5} (-x^2 v_O) \quad (\text{B.3})$$

Since we have chosen $R_5 = R_6 = R = 1\text{k}$ and $\beta_{5\text{kpot}}$ is a $5\text{k}\Omega$ potentiometer, $\beta \triangleq \beta_{5\text{kpot}}/R$. Substituting for v_O from Eq. (B.2), v_M in Eq. (B.3) can be simplified as:

$$v_M(t) = \beta(I_s i_L) + \beta x^2 (-I_s i_L) \quad (\text{B.4})$$

Upon further simplification, we get:

$$v_M(t) = -\beta I_s (x^2 - 1) i_L \quad (\text{B.5})$$

B.4. Realizing the second state equation

Applying Kirchhoff's Voltage Law around the loop with R_s and the memristor, we get:

$$v_L + v_C = v_S + v_M \quad (\text{B.6})$$

Simplifying the equation above, we get:

$$L_n \frac{di_L}{dt} = -v_C + v_M - R_s i_L \quad (\text{B.7})$$

Substituting for $v_M(t)$ from Eq. (B.5) we get:

$$\frac{di_L}{dt} = \frac{-1}{L_n} (v_C + \beta I_s (x^2 - 1) i_L + R_s i_L) \quad (\text{B.8})$$

B.5. Realizing the third state equation

Op-amps U2B and U2A realize the differential equation for the internal state $x(t)$ of the memristor. The output x of op-amp U2B is given by:

$$\begin{aligned} -C_f \frac{dx}{dt} &= -\frac{v_O}{R_b} + \frac{x}{\alpha_{10\text{kpot}}} + \frac{xv_O}{R_a} \\ \Rightarrow \frac{dx}{dt} &= \frac{v_O}{R_b C_f} - \frac{x}{\alpha_{10\text{kpot}} C_f} - \frac{xv_O}{R_a C_f} \end{aligned} \quad (\text{B.9})$$

Substituting for v_O from Eq. (B.2), we get:

$$\frac{dx}{dt} = -\frac{I_s i_L}{R_b C_f} - \frac{x}{\alpha_{10\text{kpot}} C_f} + \frac{x I_s i_L}{R_a C_f} \quad (\text{B.10})$$

B.6. Transforming circuit equations to system equations

Note that the boxed equations above are the physically scaled versions of Eq. (2). To see this, let us first define the transformations:

$$\begin{aligned} x(\tau) &= v_C(t) \\ y(\tau) &= I_s i_L(t) \\ z(\tau) &= x(t) \end{aligned} \quad (\text{B.11})$$

Note that we have mapped the internal memristor state ($x(t)$), voltage across capacitor C_f in Fig. 11) to $z(\tau)$. We also include time scaling: $\tau \triangleq T_s t = 10^5 t$. Recall $I_s \triangleq 10\,000$. Hence, we see that our circuit scales the current state variable ($y(t)$) from our system to hundreds of microamps and the time scale to tens of microseconds. This results in realizable values of inductors and capacitors.

Substituting Eq. (B.11) and the time scaling into Eqs. (B.1), (B.8) and (B.10) we get after simplifying:

$$\begin{aligned} \frac{dx}{d\tau} &= \frac{y}{C} \\ \frac{dy}{d\tau} &= \frac{-1}{L} \left(x + \beta(z^2 - 1)y + \frac{R_s}{I_s} y \right) \\ \frac{dz}{d\tau} &= -\frac{y}{T_s R_b C_f} - \alpha z + \frac{yz}{T_s R_a C_f} \end{aligned} \quad (\text{B.12})$$

Notice that since $R_s = 100\,\Omega$, $R_b = R_a = 1\,k\Omega$, $C_f = 10\,\text{nF}$, $I_s = 10\,000$ and $T_s = 10^5$, we can simplify Eq. (B.12) to the following.

$$\begin{aligned} \frac{dx}{d\tau} &= \frac{y}{C} \\ \frac{dy}{d\tau} &= \frac{-1}{L} (x + \beta(z^2 - 1)y + 0.01y) \\ \frac{dz}{d\tau} &= -y - \alpha z + yz \end{aligned} \quad (\text{B.13})$$

The values of the parameters in Eq. (B.13) can be obtained from the circuit component values:

$$\begin{aligned} C &= I_s C_n T_s \\ L &= \frac{L_n T_s}{I_s} \\ \beta &= \frac{\beta_5 \text{ kpot}}{R} \\ \alpha &= \frac{1}{T_s C_f \alpha_{10 \text{ kpot}}} \end{aligned} \quad (\text{B.14})$$

Using the component values from the circuit, we get the following values for the parameters in Eq. (B.13): $C = 1$, $L = 3.3$, $\beta = 1.7$ and $\alpha = 0.2$.

Note that in order to measure the voltage across the capacitor using the oscilloscope, we need to design another difference amplifier just like op-amp *U3B* in Fig. 11. But for this amplifier, all resistors were set to $1\,M\Omega$.

Notice that in Eq. (B.13), we have the $0.01y$ term due to the sensing resistor. Although very small, it would be useful to eliminate this resistor. A potential realization that removes this term is suggested as future work in the conclusion.

C. Experimentally Obtaining $R(x)$

In order to obtain $R(x)$, we first set v_O equal to $1\,\text{V}$ in Fig. 11. Since $v_0 = 1$, the $v_M = R(x)$. Next, we use a $1\,\text{kHz}$ $1\,\text{V}$ peak-to-peak triangle-wave as input to x . We then plot v_M versus $x(t)$ to obtain the experimental memristance curve.

D. The DC $v_M - i_M$ Curve for the Memristor

We will first mathematically derive the DC $v_M - i_M$ curve for the memristor. Consider the memristor circuit symbol below, reproduced from Fig. 1. Note that the parameters corresponding to the physical realization are $\alpha = 0.2$, $\beta = 1.7$.

To derive the DC characteristic, we first set \dot{x} equal to zero in the memristor state equation since by definition, at DC all derivatives are zero. We then solve for the internal state of the memristor in terms of current. We get:

$$\begin{aligned} -\alpha x + (1 - x)i_M &= 0 \\ \Rightarrow x &= \frac{i_M}{i_M + \alpha} \end{aligned} \quad (\text{D.1})$$

We now eliminate x in the memristor output equation using Eq. (D.1):

$$v_M(t) = \beta(x^2 - 1)i_M \quad (\text{D.2})$$

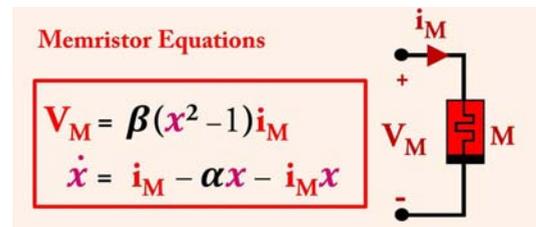


Fig. 12. The memristor used in our circuit, with $\alpha = 0.6$, $\beta = 1.5$.

Thus, the DC $v_M - i_M$ function of the memristor is given by:

$$v_M(t) = -i_M \left(-1 + \frac{i_M^2}{(i_M + \alpha)^2} \right) \beta \quad (D.3)$$

A plot of the function in Eq. (D.3) is shown in Fig. 13, with the *locally-active* region highlighted.

The significance of local activity is that this region of negative resistance is essential for chaos [Chua, 2005]. In other words, we need at least one *locally-active* element for chaos [Chua, 2005]. Our memristor is *locally-active* as well as nonlinear, hence we can make the other two elements (the inductor and capacitor) in our circuit *linear* and *passive*. Thus, when our system is chaotic, the current through and the voltage across the memristor will mostly be in the *locally-active* region of Fig. 13. This fact is also highlighted in Fig. 8. We have superimposed a few (i_M, v_M) measurements from the actual circuit on the memristor DC $v_M - i_M$ curve. We can see that most of the points do indeed lie in the *locally-active* region.

In order to plot the experimental DC characteristic in Fig. 8, we used the test circuit shown in Fig. 14.³ The current source $i_S(t)$ was configured to be approximately 10 mA amplitude sine-wave, at

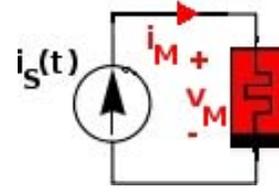


Fig. 14. A test circuit we used for plotting the memristor DC $v_M - i_M$ characteristic and the pinched-hysteresis loops.

a frequency of 0.5 Hz. We placed the oscilloscope into “persistence-mode” so that we could record the points. We then plotted v_M versus this input current on the oscilloscope.

Note that in order to plot the pinched hysteresis loop, we simply increased the frequency of the sinusoidal waveform to obtain Figs. 9(a) and 9(b).

E. BIBO Instability of Sprott’s Memristive System

Consider the system in Eq. (8), repeated below for convenience:

$$\begin{aligned} \frac{dx}{dt} &= \frac{y}{C} \\ \frac{dy}{dt} &= \frac{-1}{L}(x - zy) \\ \frac{dz}{dt} &= 1 - y^2 \end{aligned} \quad (E.1)$$

In Eq. (E.1), we will be concerned with the behavior of the memristor for a bounded input. Suppose $y(t) = \sin(\omega t)$. Substituting this function into the dz/dt equation in Eq. (E.1), we get:

$$\frac{dz}{dt} = 1 - \sin^2(\omega t) \quad (E.2)$$

The equation above is separable so it can be easily integrated (assuming zero initial conditions) using basic calculus to find $z(t)$:

$$z(t) = \frac{t}{2} + \frac{\sin(2\omega t)}{4\omega} \quad (E.3)$$

Notice the presence of the linear $t/2$ function on the right-hand side that implies the internal state $z(t)$ of the memristor is unbounded. Hence our system is BIBO unstable.

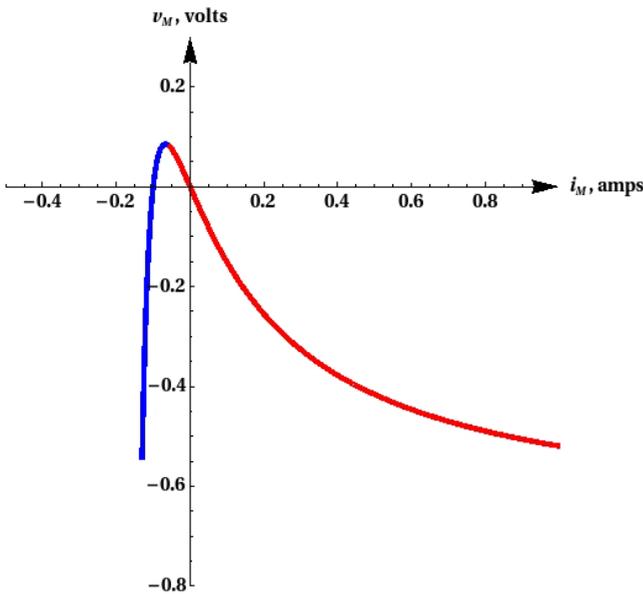


Fig. 13. The theoretical memristor DC $v_M - i_M$ curve. We have highlighted the *locally-active* region in red.

³The current waveform generator is a voltage waveform generator in series with a large resistance of 100 kΩ. By Norton’s theorem, we thus have a current source [Chua, 1969]. We thus have a current source in parallel with a 100 kΩ resistor that draws a negligible amount of current.