

# Memristor Modelling

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**Abstract**—In this paper, we show a simple circuit setup for experimentally plotting the  $v - i$  non-transversal pinched-hysteresis Lissajous fingerprint of a physical memristor - the common fluorescent gas discharge tube. The setup helped us investigate the effects of physical parasitics (inductors and capacitors) on the memristor  $v - i$ .

## I. INTRODUCTION

The memristor was postulated as the fourth fundamental circuit element by Dr. Leon O. Chua in 1971 [3]. Fig. 1 illustrates how the memristor "completes" the fundamental 2-terminal circuit elements in electrical engineering.

However, unlike a resistor, capacitor or inductor, there is a need for a physical device that aptly illustrates the unique characteristics [3] of a memristor. Although a variety of memristors [9], [7] have been identified in literature and memristor emulators [2], [6] also abound, a simple experimental setup that helps us study the  $v_M - i_M$  ( $v - i$ ) pinched-hysteresis fingerprint [3], [4] of a physical memristor, to our knowledge, is still lacking.

The purpose of this paper is to propose the simple setup shown in Fig. 2 that helps us plot the  $v_M - i_M$  curve of a fluorescent (gas) discharge tube. A youtube video of our experiment is online: <http://www.youtube.com/watch?v=hDfJoXrCSxk>

We first have to understand that a circuit model is not an equivalent circuit of a device since no physical device can be exactly mimicked by a circuit or mathematical model [5]. In fact, depending on the application (e.g., frequency of operation), a given device may have many distinct physical models [5]. There is no "best model" for all occasions. The best model in a given situation is the simplest model capable of yielding realistic solutions [5]. Thus device modelling is both an art (physical device equation formulation) and a science (nonlinear network synthesis) [5].

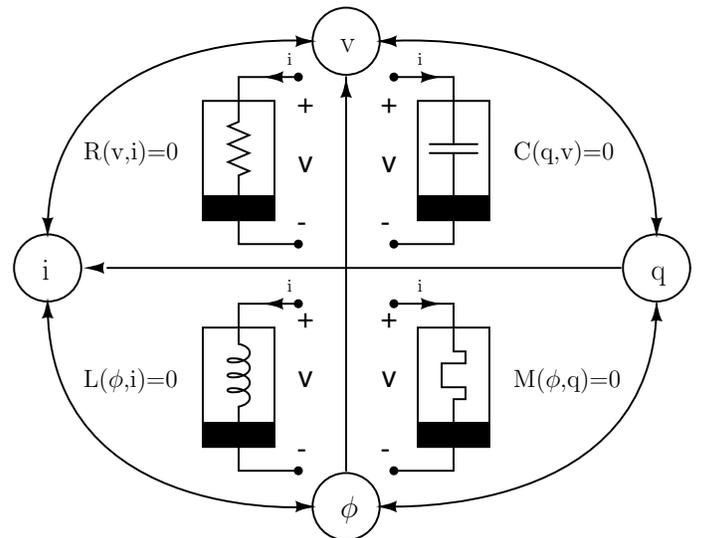


Fig. 1. The four fundamental 2-terminal circuit elements relate the fundamental circuit variables [5]. Note that current is defined as the rate of flow of charge ( $i = \dot{q}$ ). Voltage is defined as the rate of change of flux-linkage ( $v = \frac{d\phi}{dt}$ ). Flux-linkage is the number of magnetic field lines passing through a given cross-sectional area.

In the case of memristive device modeling, Theorem 1 is a must for model-validation [5].

*Theorem 1:* Under a large-signal sinusoidal current excitation, the Lissajous figure associated with the periodic voltage response  $v_M(t)$  and the excitation current  $i_M(t)$  is generally a double-valued function which passes through the origin.

However, practically, we cannot sweep the input for all frequencies and all amplitudes. Nevertheless in this paper we will show that using our setup, we are able to investigate the effects of physical parasitics (inductors and

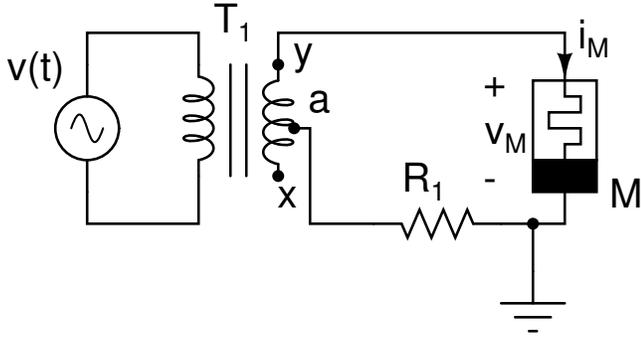


Fig. 2. Input  $v(t)$  is 120 V, 60 Hz AC. Transformer  $T_1$  is a Gaseous (Neon) Tube Transformer from Franceformer, part number 12030P, cost of the device is approximately 120 US dollars. The secondary is rated at 12 kV, 30 mA.  $R_1$  is a 0.125 W 150  $\Omega$  carbon film resistor for measuring current.  $M$  is the discharge tube, a Phillips F15T8 rated at 15 W that costs approximately 10 US dollars. Our transformer has three output terminals. One output terminal (node  $y$ ) is connected to the memristor as shown. Node  $a$  is the chassis ground terminal of the transformer that is simply connected to one end of  $R_1$  as shown. Node  $x$  is the other output terminal that is left floating. Nevertheless, node  $x$  is at  $\pm 6000$  V and hence one must observe proper safety precautions while using this setup.

capacitors) on the memristor model.

This paper is organized as follows: in the next section, we will first propose two conjectures regarding parasitics (linear inductors and capacitors) with memristors. Section 3 will show mathematical simulations of the discharge tube memristor model [4] and we will also simulate the effects of parasitics. Note that we do not discuss a resistor in series or parallel with a memristor, since the equivalent circuit is still a memristor [3]. We will then confirm our simulations by comparing to the physical experimental Lissajous figure. The paper will conclude with a discussion of future work.

## II. $v_M - i_M$ CURVE OF MEMRISTOR IN SERIES (PARALLEL) WITH INDUCTOR (CAPACITOR) PARASITIC

First, we need a definition and the memristive model of the discharge tube [4].

$$v = R(x, i)i \quad (1)$$

$$\dot{x} = f(x, i) \quad (2)$$

$$v = M(n)i \quad (3)$$

$$\dot{n} = -\beta n + \alpha M(n)i^2 \quad (4)$$

Eqns. 1 and 2 define the current-controlled memristor. Eqns. 3 and 4 are the memristive equations for a discharge tube.  $M(n) = \frac{F}{n}$ ,  $\alpha$ ,  $\beta$  and  $F$  are parameters depending on the dimensions of the tube and the gas fillings.  $n$  is the number of conducting electrons. Now, we will state the two conjectures.

*Conjecture 1:* Consider the circuit in Fig. 3. Under a large-signal sinusoidal current excitation, the  $v_M - i_M$  plot associated with the periodic voltage response  $v_M(t)$  and

the excitation current  $i_M(t)$  for Fig. 3 is un-pinned at the origin, due to a perturbation of  $v_M$  such that the following equations are satisfied:

$$i_M = 0 \ \& \ v_M > 0 \Rightarrow \dot{v}_M > 0 \quad (5)$$

$$i_M = 0 \ \& \ v_M < 0 \Rightarrow \dot{v}_M < 0 \quad (6)$$

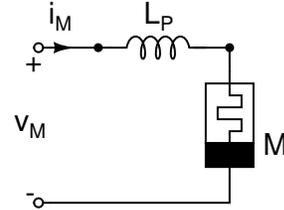


Fig. 3.  $L_p$  is parasitic inductor that is in series with the memristor  $M$ .

*Conjecture 2:* Consider the circuit in Fig. 4. Under a large-signal sinusoidal current excitation, the  $v_M - i_M$  plot associated with the periodic voltage response  $v_M(t)$  and the excitation current  $i_M(t)$  for Fig. 4 is un-pinned at the origin, due to a perturbation of  $v_M$  such that the following equations are satisfied:

$$i_M = 0 \ \& \ v_M > 0 \Rightarrow \dot{v}_M < 0 \quad (7)$$

$$i_M = 0 \ \& \ v_M < 0 \Rightarrow \dot{v}_M > 0 \quad (8)$$

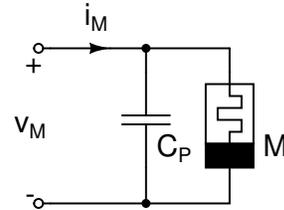


Fig. 4.  $C_p$  is parasitic capacitor that is in parallel with the memristor  $M$ .

The main concept behind Eqns. 5 and 6 (Eqns. 7 and 8) is that current lags (leads) voltage by  $\frac{\pi}{2}$  in a purely inductive (capacitive) circuit.

Therefore, the first effect of the parasitic element is that voltage and current cannot be equal to zero simultaneously and hence the equivalent hysteresis loop becomes un-pinned at the origin.

In order to obtain the inequalities, we need to understand that the  $v_M - i_M$  Lissajous figure is dynamic in the sense that one should specify both  $\frac{dv_M}{dt}$  and  $\frac{di_M}{dt}$  in the plot. We can specify these time derivatives via simulation, the subject of the next section.

## III. MATHEMATICAL SIMULATION

Results from Mathematica simulation<sup>1</sup> are shown in Figs. 5, 6 and 7. Simulation parameters were selected to

<sup>1</sup>Mathematica code is online: [www.harpgroup.org/muthuswamy/pubs/code/2014/idealAndPracticalDischargeTubeSimulations.nb](http://www.harpgroup.org/muthuswamy/pubs/code/2014/idealAndPracticalDischargeTubeSimulations.nb)

highlight salient features of the plot. It would be instructive to obtain parameters from a physical discharge tube.

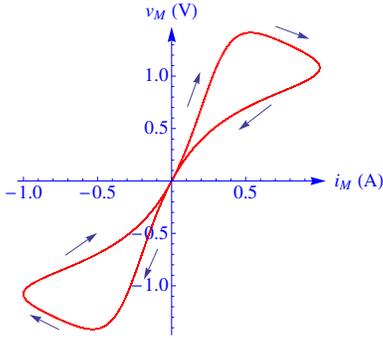


Fig. 5. Theoretical  $v_M - i_M$  memristor (discharge tube) Lissajous figure from Mathematica. Parameters used for simulation were  $\beta = 0.1, \alpha = 0.1, F = 1, \omega = 0.063$ .

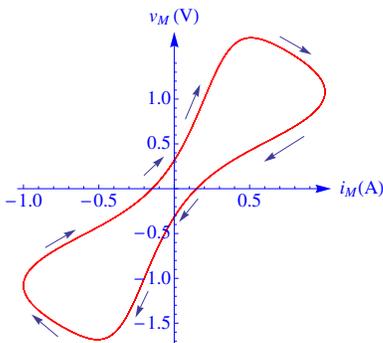


Fig. 6. Mathematica  $v_M - i_M$  for inductor in series with memristor (discharge tube). A parasitic inductance of 5 H was used, memristor parameters are the same as in Fig. 5.

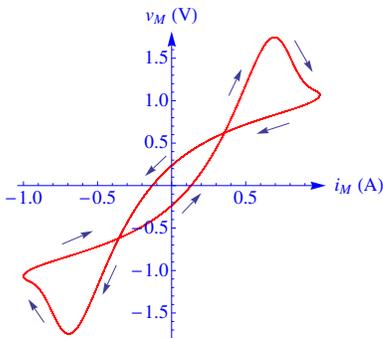


Fig. 7. Mathematica  $v_M - i_M$  for capacitor in parallel with memristor (discharge tube). A parasitic capacitance of 1 F was used, memristor parameters are the same as in Fig. 5.

Fig. 5 shows that we have a non-transversal pinched-hysteresis loop [1]. Suppose we add a parasitic inductor in series. In this case, current should start lagging voltage and we can see that effect in Fig. 6: when  $i_M = 0$ , if  $v_M > 0$ , then  $v_M$  should be increasing because voltage is leading current. Hence,  $v_M > 0$ . Similarly, when  $i_M = 0$  and  $v_M < 0$ , then  $v_M$  should continue to decrease and thus  $v_M < 0$ .

An analogous argument applies for the parasitic capacitor simulation result in Fig. 7.

#### IV. THE EXPERIMENTAL $v_M - i_M$ CURVE

We can verify our observations from the previous sections via our experimental setup in Fig. 2. First we need transformer  $T_1$  since the tube needs a high startup voltage to initiate gas discharge. The neon-tube transformer has a large output leakage inductance (1400 H measured at 60 Hz). Since the transformer output is rated at 12,000 V, 30 mA and the startup voltage of the discharge tube is only around 100 V,  $i_M(t)$  is limited to 30 mA at 60 Hz as shown in Fig. 8a. We use the standard technique of a sense resistor  $R_1$  to convert memristor current to voltage.

Since the transformer chassis at node a in Fig. 2 is floating with respect to ground, we can attach earth ground as shown in Fig. 2, to use non-floating scope probes for measurements. We reversed the  $v_M$  channel on the scope due to the passive sign convention. 10x probes were used for  $v_M$ , 1x for  $i_M$ . Figure 8 show the results.

#### V. FUTURE WORK

This paper suggested a very simple physical experiment that can be utilized even by first year undergraduate students to understand the unique properties of a memristor. The setup enabled us to study the effects of physical parasitics on memristor models. There is a plethora of future work that can be done, some of which are discussed below.

The proposed transformer is rated for 60 Hz operation. One further improvement could be to make a variable frequency input [8], to confirm other memristor fingerprints such as the decrease in hysteresis lobe area with increasing frequency [1].

We should also mathematically prove conjectures 1 and 2. Moreover, we illustrated the conjectures using a memristor that has a non-transversal pinched-hysteresis loop [1], in order to compare simulation to experimental observations. A natural extension of the work in this paper would be for memristors with transversal pinched-hysteresis loops [1]. Note also that the stated conjectures are for current-controlled memristors. We should state and prove the equivalent properties for voltage-controlled memristors [3].

On a concluding note, since this circuit involves an extremely high startup voltage for initiating gas discharge, absolute care must be taken while using this circuit. The authors (or any of their affiliates) are not responsible for any death or injury caused by using this circuit.

#### ACKNOWLEDGMENT

The authors would like to Ferenc Kovac, Dr. H. G. Gadiyar, Dr. S. Kasiviswanathan and Dr. Gerald Thomas for very productive and intellectual discussions.

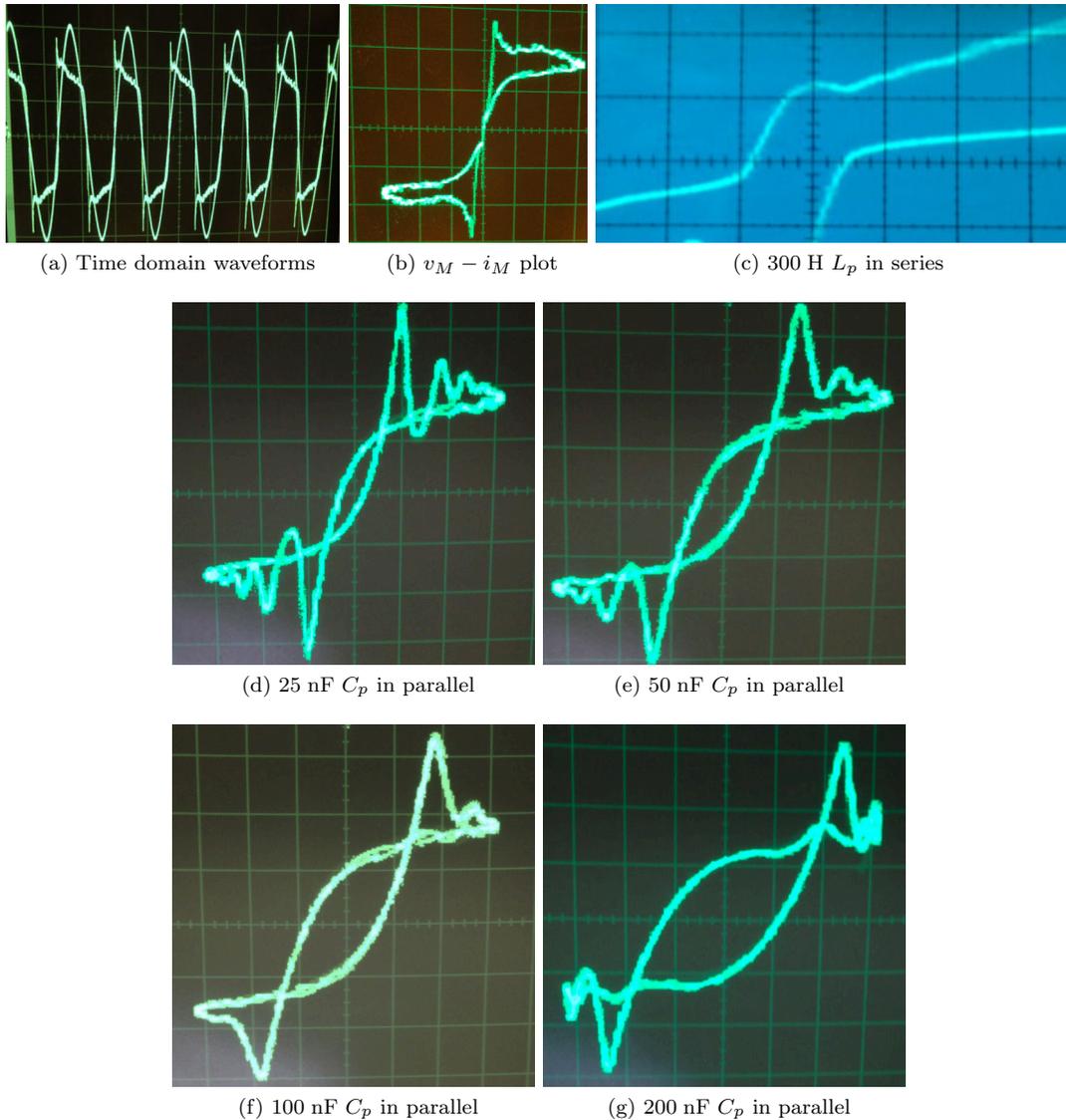


Fig. 8. Results from the physical experiment. Time-scale is 10 ms/div. The X-input ( $i_M(t)$ ) scale and Y-input ( $v_M(t)$ ) scale for Figs. 8a, 8b, 8d through 8g are 2 V/div and 5 V/div respectively. However, the Y-input to the scope uses a 10x probe. In Fig. 8a, the waveforms are  $i_M(t)$  (sinusoid at 60 Hz) and  $v_M(t)$ , Fig. 8b is the Lissajous plot of Fig. 8a. The physical setup for these figures is Fig. 2. Compare Fig. 8b to Fig. 5. Notice the non-transversal pinched-hysteresis characteristic at the origin, despite physical setup parasitics. In Fig. 8c, we have used an analog scope (for quality purposes) to take a zoomed in (X-scale is at 100 mV/div) view of the origin, with a 300 H parasitic inductor in series. We need such a large inductor to see any measurable effects without experimental error since the secondary winding of the transformer has an inductance of approximately 1400 H at 60 Hz. Figs. 8d through 8g illustrate the effect of including and systematically increasing the parasitic parallel capacitance. Notice how the expansion of the previously pinched-hysteresis loop around the origin points to the fact that the circuit is becoming "more capacitive" than memristive.

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