A Mixed-Signal EEG Interface Circuit For Use In First Year Electronics Courses

Vincent Lee*, Jennifer Monski†, Winthrop Williams*, Bharathwaj Muthuswamy‡,
Tom Swiontek‡, Michel Maharbiz*, Vivek Subramanian* and Ferenc Kovac*
*Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720
Email:{agent_lee,winthrop,ferenc}@berkeley.edu,{maharbiz,viveks}@eecs.berkeley.edu
†Department of Biomedical Engineering
Milwaukee School of Engineering, Milwaukee, WI 53202
Email:monskij@msoe.edu
‡Department of Electrical Engineering and Computer Science
Milwaukee School of Engineering, Milwaukee, WI 53202
Email:{muthuswamy,swiontek}@msoe.edu

***Abstract*— In their first electronics course, many students find operational amplifiers, analog filters and sensor interface circuitry perplexing and daunting. The purpose of this paper is to present a circuit that addresses these pitfalls. A simplified electroencephelogram (EEG) circuit that is interfaced to a digital backend is proposed. The completed circuit involves using instrumentation amplifiers and filters for the EEG interface. The digital backend helps analyze EEG data on the computer.**

I. Introduction

Typical students in the Circuits and Systems (CAS) track have difficulty in relating abstract concepts such as transfer functions to practical systems like amplifiers and filters. In systems courses, students are usually asked to obtain Bode plots from transfer functions. In circuits courses, students are asked to "design an active low pass filter with 40 dB gain in the passband and -20 dB/decade rolloff starting at 30 Hz". The student asks natural questions such as "how do I translate a Bode plot to a physical system?", "how do I choose a rolloff frequency?" and "why choose 40 dB gain and not 60 dB?". Hence the goal of this paper is to enhance CAS education by proposing a circuit that is appropriate as a project for a first year electronics course. By first year electronics course, we are referring to any course in which the students have exposure to basic DC and AC circuit theory.

The problem addressed in this paper is EEG interfacing. The learning outcome of this project is for the student to be able to interface to a noisy, very low amplitude biological signal [4]. The design constraints are:

1) Interface to signals with very low (tens of microvolts [4]) signal amplitudes. The pertinent EEG waveforms to be visualized are alpha waves.
2) Filter 60 Hz line noise. The alpha waves have a frequency range of 8 Hz to 13 Hz [4]. Thus the filtering circuit passband should be at least 13 Hz. Note that if the line frequency is 50 Hz, the notch filter can be adjusted to accommodate this frequency.
3) Provide electrical isolation for safety reasons.
4) Confirm that EEG signals have been obtained.

Constraints 1 through 3 in the list are addressed via appropriate analog circuits. Constraint 4 is addressed by using a digital backend for implementing a fast Fourier transform (FFT). Thus the project is a mixed-signal design that incorporates both analog and digital subsystems. The crux of this paper is a discussion of the analog subsystems shown in Fig. 1.

This paper is organized based on the different project subsystems shown in Fig. 1. The amplification subsystem is first discussed and this consists of an instrumentation amplifier front-end and a second gain stage. Next 60 Hz line noise is reduced. This is achieved by the very high common mode rejection ratio (CMRR) from the instrumentation amplifier and cascaded notch filters. These notch filters are simply RLC circuits but a gyrator [1] is used to emulate a 26.5 H inductor at 60 Hz. To further reduce 60 Hz noise, the analog components are driven by $\pm$ 5 V regulators that are in turn powered by $\pm$ 9 V batteries. The final analog stage is an ISO122 galvanic isolation amplifier [11]. Section V shows experimental results. A LabVIEW based platform is used for the digital backend, to experimentally measure and classify the EEG waveform into different frequency bins. Since post processing is a must to interpret EEG waveforms, the LABVIEW VI is available online [13]. The paper concludes by discussing project deployment and future work.

II. Amplifying Microvolt Signals

Since the range of signal amplitude is approximately 50 μV [4], a DC gain of approximately 100,000 would be ideal. This gain would factor into a gain of 1000 from the instrumentation amplifier and a gain of 100 from the second stage. However for some electrodes, saturation of

978-1-4673-0219-7/12/$31.00 ©2012 IEEE

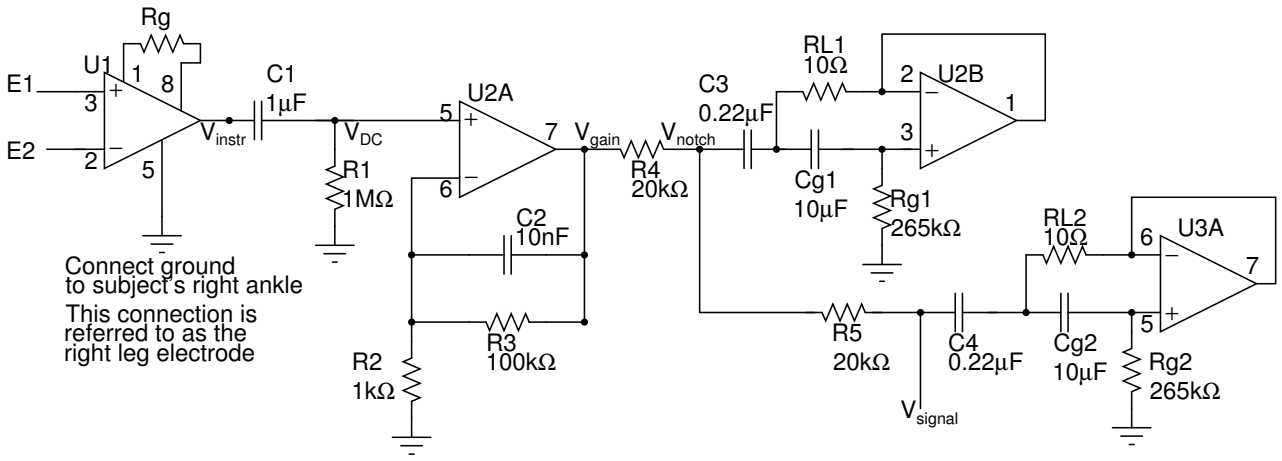

Fig. 1: The analog subcircuits for the mixed-signal EEG interface. The instrumentation amplifier U1 is an INA114, the operational amplifiers U2 and U3 are TLC277s. Since a discussion of transfer functions are included in first year electronics courses, the student is asked to derive theoretical transfer functions for the associated analog subsystems. For clarity purposes, the power supplies and isolation circuits are not shown.

the instrumentation amplifier was observed because of the very small (tens of mVs) voltage differences between the electrodes. Reducing the gain of the instrumentation amplifier front end resolved this issue. Hence pick a gain of 100 for the instrumentation amplifier and 100 for the gain stage. Note that other combinations of gain values are also possible, the limiting factor is instrumentation amplifier saturation. However, the first stage must be an instrumentation because of the high common mode rejection ratio (CMRR) required for amplifying very low amplitude signals.

A. The Instrumentation Amplifier Front-End

The instrumentation amplifier is a Texas Instruments INA114 [5]. The gain of this instrumentation amplifier stage is given by Eq.(1)

$$\frac{\mathsf{V_{instr}}}{\mathsf{E1-E2}} = 1 + \frac{50k\Omega}{\mathsf{Rg}} \tag{1}$$

$\mathsf{E1}, \mathsf{E2}$ are connected to the electrodes. The ground of the instrumentation amplifier is connected to the subject's left ankle, and to the common ground of the circuit. This is necessary to make sure the subject is not floating with respect to the circuit reference.

Choosing a gain of 100 for the instrumentation amplifier for EEG, the value of Rg (nearest 1% tolerance) obtained from the datasheet [5] is highlighted in Eq.(2).

$$\boxed{\mathsf{Rg} = 511\ \Omega} \tag{2}$$

Note that the value of R_g above corresponds to a gain of 98.8. It is important that Rg have a tolerance of $\pm 1\%$ [5] to minimize noise contributions from the gain resistor itself.

B. The Gain Stage

The gain stage is U2A in Fig. 1 and is a non-inverting amplifier [3]. All operation amplifiers are TLC277CP [12]. The DC transfer function of this stage is given by Eq.(3).

$$\frac{\mathsf{V_{gain}}}{\mathsf{V_{DC}}} = 1 + \frac{\mathsf{R3}}{\mathsf{R2}} \tag{3}$$

Eq.(3) is obtained by understanding that the capacitor $\mathsf{C2} = 10\ nF$ acts like an open-circuit at DC because of its very high impedance. In Fig. 1, R2 is a $5k$ linear potentiometer that is set to $1k\Omega$. Hence using the parameter values for U2A from Fig. 1 in Eq.(3), a DC gain of 101 is obtained from U2A.

Thus the net DC gain from the amplifier subsystem is the product of Eq.(1) and Eq.(3). Using the parameter values from Fig. 1, Eq.(4) is obtained for the total DC gain.

$$\boxed{98.8 \times 101 = 9978} \tag{4}$$

A gain of 9978 implies that a 50 μV signal would be amplified to approximately 0.5 V.

III. Filtering 60 Hz Line Noise

A. Instrumentation Amplifier

The common mode rejection ratio is a measurement used to gauge the differential gain of an amplifier against its common mode gain [4], Eq.(1).

Utilizing an instrumentation amplifier with a high common rejection ratio in the first stage significantly decreases the 60 Hz noise in the signal. To measure the common mode rejection ratio of the instrumentation amplifier, the differential gain of the amplifier was first measured at a given frequency (60 Hz); next, the inverting and non-inverting inputs of the instrumentation amplifier were shorted together, such that only common mode voltage was extending into the amplifier. For this testing, an

Aglient 33120A function generator was used due to its ability to generate small amplitude signals when examining difference mode (to prevent saturation of the instrumentation amplifier) and also large amplitude signals for examination of the common mode gain. The CMRR result is shown in Eq.(5).

$$CMRR = 20\log_{10}\frac{A_d}{|A_{cm}|} = 20\log_{10}\frac{98.8}{A_{cm}} \approx 110\ dB \quad (5)$$

B. DC blocker

Although the DC blocker is not part of the 60 Hz filtering circuit, it filters DC offset voltages that propagate through the instrumentation amplifier. This is evident from Eq.(6) that shows the transfer function of the DC blocker (simplified using component values).

$$\frac{\mathbf{V_{DC}}(s)}{\mathbf{V_{instr}}(s)} = \frac{s}{s+\frac{1}{\mathsf{R1C1}}} = \frac{s}{s+1} \quad (6)$$

The frequency response of the gain stage is only apparent at high frequencies because of the 10 nF capacitor in Fig. 1. But probably the most important filtering circuit is the notch filter, the topic of the next subsection.

C. The Notch Filter

The notch filter provides additional 60 Hz filtering. The RCL model of one notch filter[1] in Eq.(9) shown in Fig. 2.

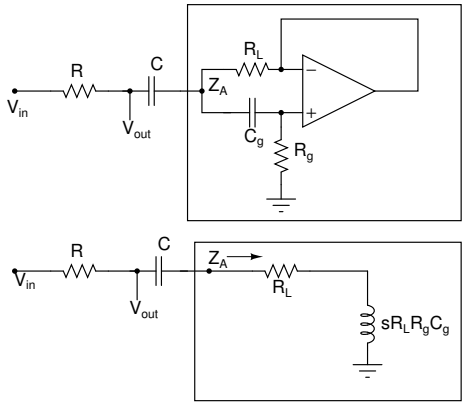

Fig. 2: An RCL notch filter. The inductor is realized using an operational amplifier based gyrator or impedance inverter.

The active operational amplifier based circuit in Fig. 2 at node A has an impedance given by Eq.(7).

$$\mathbf{Z_A}(s) = \mathsf{R_L} + s\mathsf{R_L}\mathsf{R_g}\mathsf{C_g} \quad (7)$$

Hence the operational amplifier circuit realizes an inductor with $\mathsf{L} = \mathsf{R_L}\mathsf{R_g}\mathsf{C_g}$ and series resistance $\mathsf{R_L}$.

[1]The second notch filter in Fig. 1 has the same transfer function as the first. A second notch filter is used for more attenuation of line noise.

Now, the transfer function of the second circuit in Fig. 2 given by Eq.(8) (assuming $\mathsf{R_L} = 0$).

$$\frac{\mathbf{V_{out}}(s)}{\mathbf{V_{in}}(s)} = \frac{\frac{1}{s\mathsf{C}} + s\mathsf{L}}{\mathsf{R} + \frac{1}{s\mathsf{C}} + s\mathsf{L}} \quad (8)$$

For the parameter values in Fig. 1, $\mathsf{R_L} << \mathsf{R_g}$ and hence the assumption that $\mathsf{R_L}$ can be neglected is valid. Also, $L = (10\ \Omega)\cdot(265\ k\Omega)\cdot(10\ \mu F) = 26.5\ H$. For an excellent description of why such a large inductor value is needed, please refer to [2].

Using the parameter values from Fig. 1 the transfer function of the first notch filter is shown in Eq.(9).

$$\frac{\mathbf{V_{notch}}(s)}{\mathbf{V_{gain}}(s)} \approx \frac{s^2 + 171527}{s^2 + 754.7s + 171527} \quad (9)$$

D. Bode Plot

The Bode magnitude plot of $\frac{\mathbf{V_{signal}}(s)}{\mathbf{E1-E2}(s)}$ from Fig. 1 is shown in Fig. 3. Both simulation[2] and experimental data are plotted.

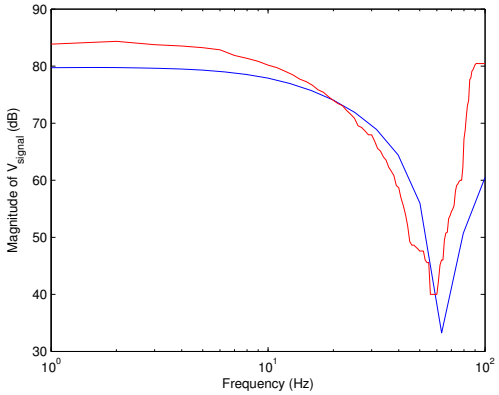

Fig. 3: The simulation bode plot (blue) versus the experimental bode plot (red). Simulation was carried out using MultiSim [8] (a SPICE [10] graphical front end). Experimental data was obtained by using a 80 dB attenuator to input a 100 μV sinusoid with varying frequency and then measuring the amplitude of the output.

E. Power Supply

In order to avoid line noise from the DC power supplies, the LM7805 [6] regulator for 5 V and LM7905 [7] for $-5\ V$ were used; dual supplies are used for larger output swing. The regulators are driven by $\pm 9\ V$ batteries. 0.1 μF filter capacitors were used at regulator outputs for stability and further filtering. The circuit should either be driven by batteries or an isolated supply for safety reasons and for minimizing line noise.

[2]For SPICE simulations, please set the transient iteration limit to 1000 and DC iteration limit to 2000 to avoid convergence errors.

IV. Electrical Isolation

Due to the nature of obtaining signals from human subjects, an isolation system was needed within the amplifier system. For this, an ISO122 isolation chip was used. Essentially, the isolation chip establishes a secondary ground for the system, thus preventing any current flow from devices receiving AC outlet power, such as an oscilloscope, from entering a the human subject. Hence the isolation chip was placed after the second notch filter.

V. Experimental Results

Once the frequency response of the circuit has been experimentally verified, biopotential data can be obtained. Fig. 4 shows FFT data from LABVIEW, the EPS figure was generated using MATLAB for clarity.

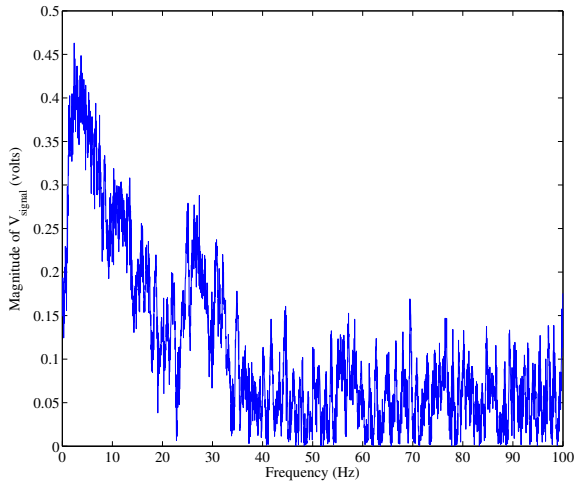

Fig. 4: A snapshot of the EEG FFT from LabVIEW, captured using NI-myDAQ [9]. Electrodes were placed on the occipital lobe at the base of the skull. Reference electrode was placed on top of the head. The subject should be in a sitting position and slowly close their eyes. Another individual would notice alpha wave activity in the 8 - 13 Hz range, namely, the FFT should distinctly increase in dB within this frequency range. Note that the subject should be still or muscle movement will disturb the notch filter. The recovery time of the notch filer is on the order of a few seconds because of the 26.5 H inductor emulation.

VI. Conclusions and Future Work

A robust circuit for EEG interfacing has been presented. After going through this project, a typical CAS student should have solid understanding of instrumentation amplifiers, filters, protection circuitry and isolation.

At the University of California, Berkeley this circuit is being implemented as the course project in the Fall 2011 (September through December) offering of EECS 40 (the introductory microelectronics course) by Prof. Maharbiz. It is also being implemented in EECS 100 (introduction to electrical engineering for non-EE majors) by Prof. Subramanian. The varied background of the students suggest that the circuit is robust enough for modifications. Specific modifications include a printed-circuit-board implementation in EECS 40 and also the use of an active driven right leg [4]. Protection circuitry is also implemented at the inputs to the instrumentation amplifier. In EECS 40, students are also asked to design the instrumentation amplifier front-end out of three discrete operational amplifiers (TLC277s). At the Milwaukee School of Engineering (MSOE), this circuit is being considered for use in EE2070 (Linear Circuits - Transients), the final course in the basic circuits curriculum.

Unlike the ECG that is readily obvious in the time domain, EEG waveforms require quite a bit of work before they can be correctly identified. Future work involves using this circuit as the front-end to devise an EEG "present" or "absent" test that does not involve a Fast Fourier Transform. Note that since this circuit involves interfacing with a living organism, absolute care must be taken while using this circuit. The authors (or any of their affiliates) are not responsible for any harm or injury caused by using this circuit.

Acknowledgment

The authors would like to thank Dr. John Gassert, Dr. Larry Fennigkoh, Dr. Ron Gerrits (MSOE), Ming Wong, Dr. Stephen Derenzo (UC Berkeley) for all their help and support. This project would not have been possible without the countless hours of testing by the Fall 2011 EECS 40 and EECS 100 teaching assistants at the University of California, Berkeley. Many thanks to Texas Instruments for their generous donation of components and National Instruments for their generous donation of myDAQ hardware.

References

[1] D. F. Berndt and S .C. Dutta, "Inductor Simulation With a Unity Gain Amplifier", *IEEE Journal of Solid State Circuits*, **SC-4**, pp. 161-162, 1969.

[2] H. Liu, J. Kotker, and B. Ayazifar, "A first lab in filter design: Power line hum suppression in an ECG signal," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, pp. 2812 -2815, 2010.

[3] J. W. Nilsson and S. Riedel, *Electric Circuits*, 8th ed. New Jersey:Prentice-Hall, 2007.

[4] J. G. Webster, *Medical Instrumentation : Application and Design*, 3rd ed. New York City, New York: Addison-Wesley, 1998.

[5] *INA114 Datasheet*, Burr-Brown and Texas Instruments, 1998.

[6] *LM7805 Datasheet*, Fairchild Semiconductor, 2011.

[7] *LM7905 Datasheet*, Fairchild Semiconductor, 2011.

[8] *MultiSim Circuit Simulation Program*, National Instruments, 2011. [Online]. Available: `http://www.ni.com/multisim/`

[9] *NI-myDAQ*, National Instruments, 2011. [Online]. Available: `http://www.ni.com/mydaq/`

[10] *SPICE - Simulation Program with Integrated Circuit Emphasis*, University of California Berkeley, 2011. [Online]. Available: `http://bwrc.eecs.berkeley.edu/classes/icbook/spice/`

[11] *ISO122 Datasheet*, Texas Instruments, 1993.

[12] *TLC277 Datasheet*, Texas Instruments, 2002.

[13] *LABVIEW EEG VI*, Designed by Williams, Winthrop. [Online]. Available: `http://myweb.msoe.edu/muthuswamy/labviewEEG/`